FAIRCHILD SEMICONDUCTOR

THE ECL HANDBOOK

JULY 1974

THE ECL HANDBOOK

ECL USERS GUIDE
ECL PRODUCT INFORMATION

**Digital Systems and Applications Department,
in cooperation with the Digital Product Planning Staff,
Fairchild Semiconductor**

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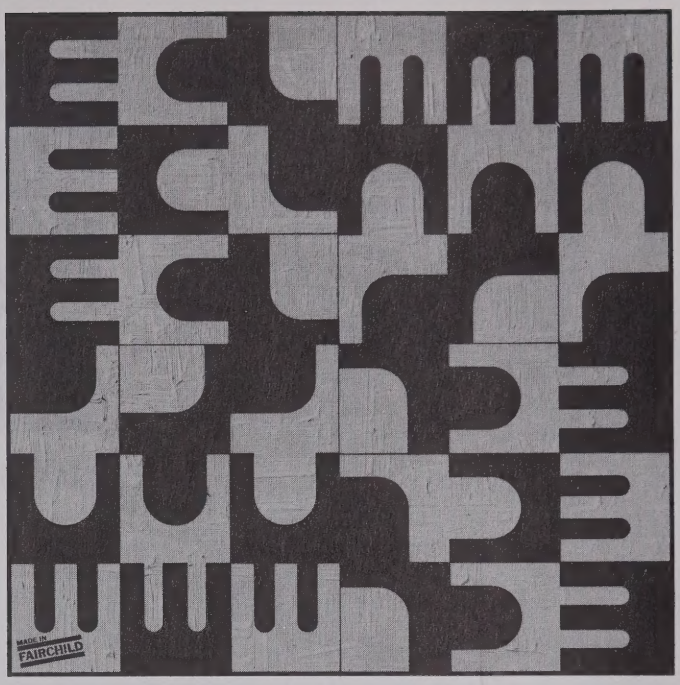

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F10K Voltage Compensated ECL Series 7

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ECL USERS GUIDE

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INTRODUCTION

Most systems in operation today use TTL logic circuits. The continuing pressure for higher performance in these systems has been satisfied, in part, by the designer's ingenuity in partitioning and, in part, by selective substitution of faster TTL elements. Eventually, however, the point is reached where the extremely fast rise times cause coupling problems; the rapid current changes cause excessive impulse voltages across ground inductances; and simple interconnect wires exhibit dynamic impedance and noticeable propagation delay. At this point, some drastic rethinking is in order with due consideration for better packaging, controlled interconnection characteristics, impedance matching, and logic circuits designed for such an environment . . . which brings us to the subject of this handbook, ECL.

Emitter Coupled Logic (ECL) has long been used in mainframe computers, wherein the fastest possible switching rates translate almost directly into system performance and sales. More recently, ECL usage has expanded into a broader range of applications, including those listed in the table below.

Although ECL integrated circuits have been available for a decade, their characteristics are relatively unfamiliar to many designers. A broad view of F10K and F95K ECL characteristics is given in Chapter 1, which summarizes the key features, compares them with TTL, and points out their advantages in high speed systems. Also listed are the extra advantages of temperature and voltage compensated ECL, which make the designer's task much easier and extend the useful lifetime of a system.

Systems tend to pass through the development stage and reach production more quickly and easily when the designer is familiar with circuit input thresholds and output voltages, what determines their values, and how they are affected by supply voltage and temperature environment. Chapter 2 discusses the various internal subcircuits and their influence on circuit characteristics. It also contains a sample analysis of noise margin deterioration with adverse conditions of supply voltage regulation, distribution gradients, temperature, and voltage drops along the ground distribution.

Communications	Instrumentation	Peripherals
Error detection and correction	Signal generators	Add-on memories
High speed modems	Correlators	Memory control systems
Signal processors	Frequency meters	Fast Fourier processors
Data compression	Counting/timing circuits	Dedicated computers
Digital filters	Frequency synthesizers	Preprocessors
Phase-locked loops	A/D converters	

INTRODUCTION

The designer who is accustomed to forming complex functions with TTL NAND gates may, for a time, be ill at ease with ECL gates. Chapter 3 gives representative examples of duplicating TTL gate functions with ECL. Also included is a sample conversion of a TTL network to ECL, first by brute force substitution then again by more judicious use of ECL capabilities. The latter conversion is more efficient in terms of logic levels, interconnections, and package count, illustrating how ECL versatility affords greater range for the designer's ingenuity. A comparison chart in Chapter 3 illustrates that ECL/MSI functions are quite similar to TTL elements.

In high speed systems, the inductance, capacitance, and signal delay along interconnections cannot be ignored. The only practical way of dealing with these factors is to treat interconnections as transmission lines. Chapter 4 reviews briefly the concept of characteristic impedance and propagation constant and discusses termination mismatch, reflections and the types of waveforms to be expected in the various combinations of overtermination and undertermination at each end of a line. The relationships between rise time, line delay, and ringing are also discussed. All sample calculations and waveforms are normalized to a 1 V signal swing, which makes the quantitative results easier to understand and adapt to any logic circuit family.

In the early days of digital ICs, many designers tried ECL, only to become frustrated and give up when they couldn't get their breadboards to operate properly. From these experiences, there developed a general impression that ECL is prone to oscillation; indeed, statements to this effect still appear in print occasionally. Continued efforts, using better test equipment and distributed circuit theory, have shown that the interaction between high speed circuits and their interconnections is the decisive factor, previously overlooked. Chapter 5 extends the transmission line approach to the specific configurations, signal levels and parameter values of 10,000 ECL. Various methods of driving and terminating signal lines are discussed, along with their advantages and limitations. Specific guidelines and recommendations are based on assumed worst case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

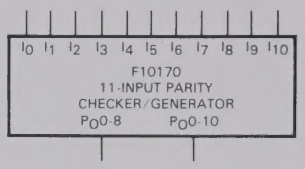
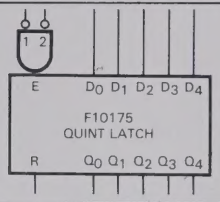
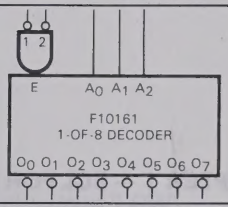
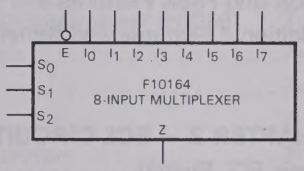
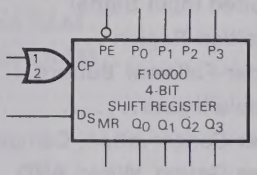
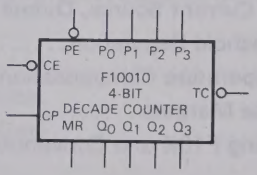
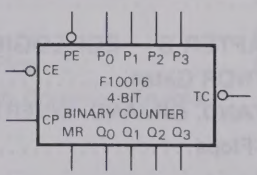
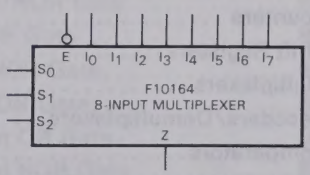
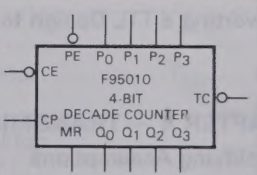
Power consumption and heat dissipation are necessarily greater with high speed circuits, due partly to circuit power drain and partly to dissipation in terminations. The increased supply currents, compared to medium speed circuits, place extra emphasis on the voltage drop along power distribution busses, including ground busses. Chapter 6 discusses methods of calculating bus resistances and estimating ground drops, and suggests general considerations regarding the relative location of communicating logic boards. Also discussed are power supply decoupling and system cooling requirements.

For convenience, a Product Information section is incorporated, making up the latter part of this handbook. Data sheets for available SSI, MSI and memory circuits are included, for both the F10,000 series and the fully compensated F95,000 series. A list of definitions of terms and symbols is also incorporated in this section.

Logic symbols used throughout the handbook follow the positive True option of MIL-STD-806B. Symbols with unique shapes are used for the simpler functions, *e.g.,* NOR, OR, NAND, AND. MSI elements are represented by rectangular blocks with appropriate external gate symbols when necessary. A small circle at an external input means that the specific input is active LOW; *i.e.,* it produces the desired function, in conjunction with other inputs, if its voltage is the lower of the two logic levels in the system. A circle at the output indicates that when the function designated is True, the output is LOW. Generally, inputs are at the top and left and outputs appear at the bottom and right of the logic symbol. An exception is the asynchronous Master Reset in some sequential circuits which is always at the left bottom corner.

Inputs and outputs are labeled with mnemonic letters as illustrated in the table opposite. Note that an active LOW function labeled outside of the logic symbol is given a bar over the label, while the same function inside the symbol is labeled without the bar. When several inputs or outputs use the same letter, subscript numbers starting with zero are used in an order natural for device operation.

LABELING FOR ECL INPUTS AND OUTPUTS

LABEL	MEANING	EXAMPLE
I_X	General term for inputs to combinatorial circuits.	
J,K S,R D P	Inputs to JK, SR, and D flip-flops, latches, registers, and counters.	
A_X, S_X	Address or Select inputs, used to select an input, output, data route, junction, or memory location.	
E	Enable, active Low in most cases.	
PE	Parallel Enable, a control input used to synchronously load information in parallel into an otherwise autonomous circuit.	
MR	Master Reset, asynchronously resets all outputs to zero, overriding all other inputs.	
CP CE	Clock Pulse, generally a High-to-Low-to-High transition. An active High clock (no circle) means outputs change on Low-to-High clock transition. Count Enable inputs for counters.	
Z_X, O_X, F_X	General terms for outputs of combinatorial circuits.	
Q_X TC	General term for outputs of sequential circuits. Terminal Count output (1111 for up binary counters, 1001 for up decimal counters).	

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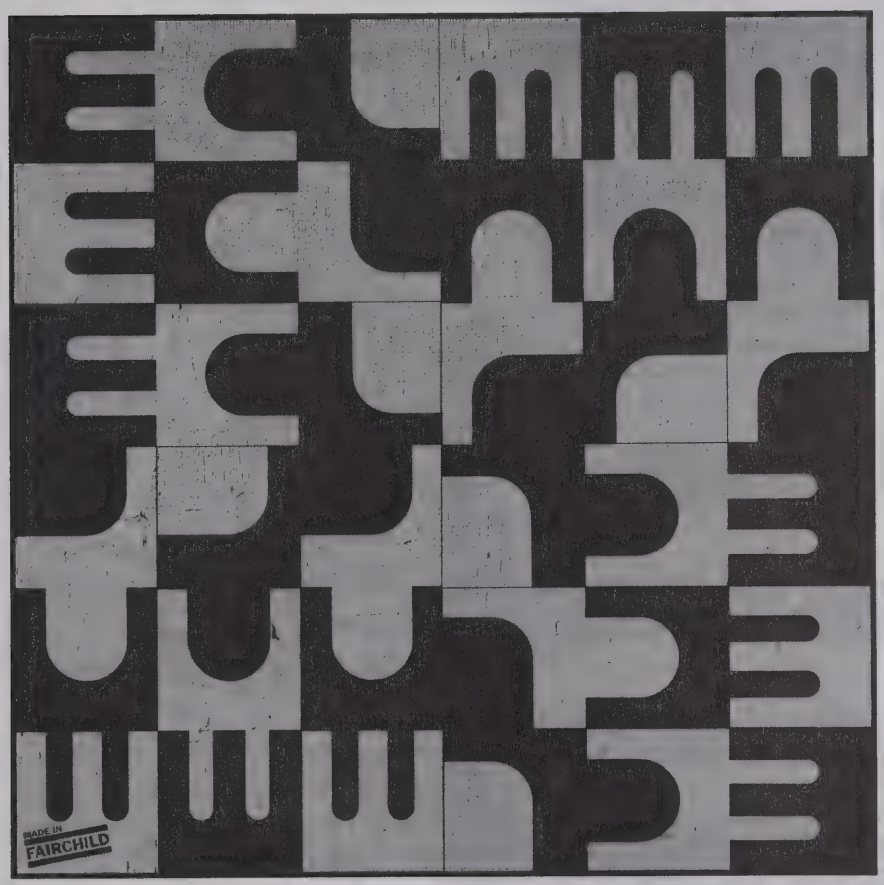
by Charles H. Alford



A designer embarked on a quest
For circuits that beat all the rest,
Followed guidelines he took
From this ECL book;
Now his high speed system's the best.

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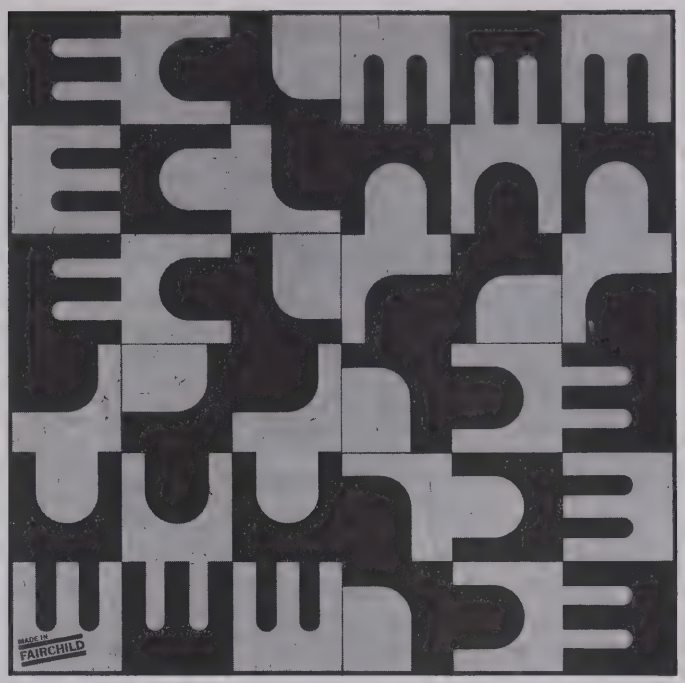

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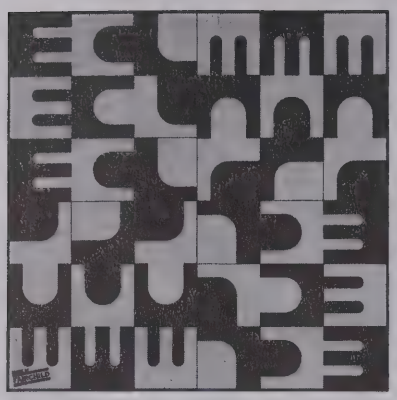

CHAPTER 1

- F10K and F95K Features and Characteristics
- Additional Features and Benefits of F95K

ECL FOR HIGH PERFORMANCE SYSTEMS

INTRODUCTION

ECL circuits incorporate features and capabilities that system designers have found offer significant advantages in high speed digital systems. These include high switching rates with moderate power consumption, short propagation delays with slow edge rates, ability to drive low impedance interconnections, compatibility with various termination methods, and wired-OR capability.

- **10,000 Series ECL** is an industry accepted, multiple-sourced ECL line offering a broad range of SSI, MSI, memory and interface elements.
- **95,000 Series ECL** is fully compensated for temperature and supply voltage variations, and offers the same functions, pinouts and operating speeds as 10,000 Series.

F10K AND F95K FEATURES AND CHARACTERISTICS

F10K and F95K features and characteristics that are particularly advantageous in high speed systems can be summarized as follows.

Low Propagation Delays

With typical delays of 2 ns for gates and 3 to 6 ns for arithmetic operations, total propagation time through a series of ECL elements is only half as much as the delay through an equivalent string of the fastest TTL elements. Similarly, ECL counters, registers and flip-flops can operate with input frequencies in the 200 MHz range. Exclusive of wiring delays, ECL thus allows clock rates twice as fast as those obtained with other forms of logic.

Slow Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughput times. Slower rise times minimize ringing and reflections on interconnect wiring and simplify physical design. Typical edge rate for F10K ECL is 200 mV per ns; in comparison, the edge rate for Schottky TTL is typically six times greater.

Wired-OR Capability

ECL outputs can be wired together, where wiring rules permit, to form the positive True OR function thus achieving an extra level of gating without extra packages. The same technique permits data bussing and party line operations.

Complementary Outputs

Many ECL elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

Low Output Impedance, High Current Capability

As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds. Since the distributed parameters cause the wiring to exhibit impedances in the 50 to 250 Ω range, signal edges are attenuated by the voltage divider action between the circuit output impedance and the wiring impedance.

Voltage mode circuits have a HIGH state output impedance of 50 to 150 Ω and thus exhibit an output step of about half that exhibited at low speeds, while ECL output impedance of 7 Ω assures a complete signal into the wiring impedance. Also, ECL outputs are fully specified for driving a 50 Ω load and have a rated output current capability of 50 mA; they can thus supply the quiescent current required for resistive terminations.

Convenient Data Transmission

The complementary high current outputs of standard ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common Mode Noise Rejection

Differential line receivers provide common mode noise rejection of 1 V or more for induced and ground noise. Differential receiving requires less signal swing than single-ended and is thus capable of restoring attenuated signals.

Constant Supply Current

The supply current drain of an ECL element is governed principally by one or more internal constant current sources, which supply operating currents for differential switches and level shifting networks. Since the current drain is the same in either state of the switches, ECL circuits are constant current loads on the supply.

Low Power Loss In Stray Capacitance

High frequency switching often consumes appreciable power when charging and discharging parasitic capacitance. Energy is consumed each time a capacitance is charged or discharged, so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance is an order of magnitude less than with TTL.

Low Noise Generation

Power supply lines are not subjected to the large current spikes common with TTL circuits. ECL does not use a totem pole output structure, thus is free of internally generated spikes. Current spikes caused by charging and discharging stray capacitance are much smaller with ECL because of the lower signal swing and slower rise time, compared to high speed TTL.

Low Crosstalk

Since induced signals are proportional to signal swings and rise times, the lower signal swings and slower rise times of ECL result in low crosstalk levels.

Voltage Variation Insensitivity

F10K and F95K ECL parameters are insensitive to supply voltage variation. As a result, requirements are relaxed on

power supply ripple, regulation, and distribution without sacrificing noise margins or operating speeds. ECL systems can tolerate greater variations in ac power levels, power supply regulators can be simpler and less expensive, and the physical arrangement of the dc distribution busses can be simplified.

ADDITIONAL FEATURES AND BENEFITS OF F95K

The Fairchild F95K ECL line adds temperature and voltage compensation to the 10,000 Series functions, pinouts and nominal speeds. This gives F95K all the advantages of the 10,000 Series ECL as well as the following added features and benefits.

Easier Engineering

Designers have more confidence that the performance characteristics observed in small scale hook-ups on the lab bench will apply in the different environments expected in prototypes, in production versions, and in field operation. Considerably less effort is expended in estimating all possible extremes of temperature and supply voltage to be expected in the final system, and translating these environmental extremes into worst case variations of output levels and input thresholds, rise times and ringing, signal swing and reflections, propagation delay and timing skew, etc. Similarly, less effort is required to design both a workable power supply regulation/distribution system and an effective cooling system.

Reduced Design Time

The time required from initial development to production start-up is greatly reduced. The reduction in time required for worst case considerations, the simplification of the power system, and relaxed cooling requirements all contribute to a shorter, and therefore less expensive development cycle.

Temperature Variation Insensitivity

The complex cooling systems required to preserve noise margins, maintain speed, and control signal swings of conventional ECL are not required with F95K ECL. Output level specifications for the F95K series elements apply over the entire temperature range and the specified noise margins assume an ambient temperature gradient of ±75°C between one circuit acting as a signal source and another circuit receiving the signal. Thus a simpler and less costly cooling system can be used and still achieve an error-free system with high performance.

High Performance

The regulation and control of dc and ac parameters achieved by F95K ECL assures that signal timing and propagation delays in critical paths are insensitive to changes or gradients of temperature and supply voltage. Guardbands can be much narrower, yet provide a higher degree of confidence, due to the elimination of skew between output levels at one location and input thresholds at another. The consistency of response and security of noise margins permit operation at higher clock rates, increasing system performance.

Easier Component Testing

There is no prolonged period of waiting for thermal stabilization nor any need for a complex cooling set-up to correlate with data sheet specifications when testing F95K ECL. Thus, incoming inspection testing is easier, faster, and the results more meaningful. Testing is accomplished at lower cost and greater effectiveness throughout the production lifetime of systems using F95K ECL.

Easier Debugging

Debugging is simplified and proceeds more rapidly in prototype development, production testing and in field operation. When a cabinet or other enclosure is opened for access in debugging, the resultant change of thermal conditions has no effect on F95K ECL. Signal swings, propagation delays, edge rates and noise margins do not change, thus the altered temperature conditions do not make existing problems disappear nor create new ones.

Lower Manufacturing Costs

Savings continue to accrue during the production lifetime of the equipment, due to the less expensive power supply and cooling systems, simplified assembly of the power bussing system, easier testing of components, card assemblies, and subsystems, easier debugging, and overall reduction in manufacturing throughput time.

Less Field Service

The broader tolerance to ac power fluctuations and ambient temperature conditions in the field minimizes service calls. When field maintenance or calibration is required, procedures are simplified and less time consuming for the same reasons that make debugging easier.

More System Sales

Shorter design time places the system on the market sooner, permitting faster recovery of investment. Higher performance plus the built-in tolerance to a wider range of installation environments broadens application areas, providing a larger potential market. Lower manufacturing costs make the system competitive over a longer period of time.

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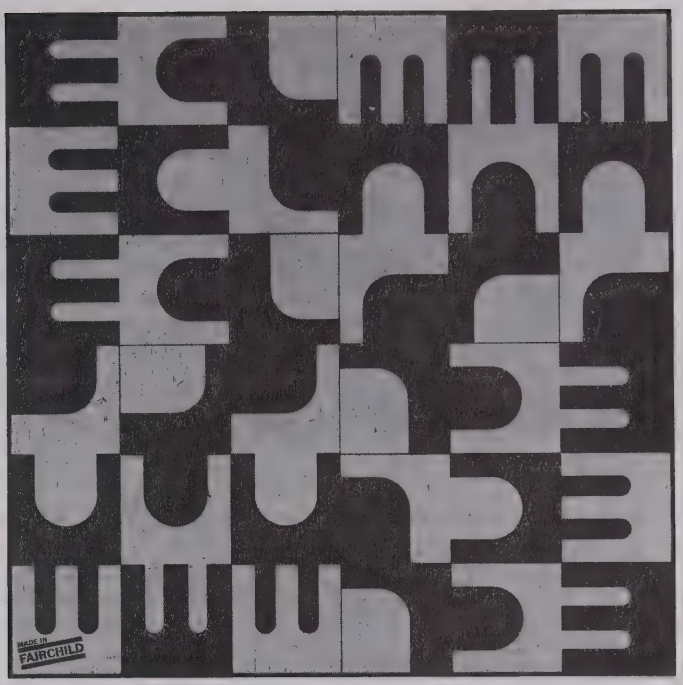

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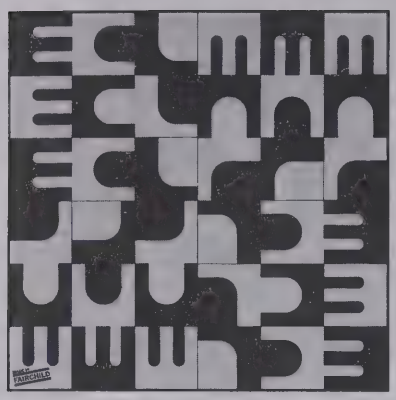

CHAPTER 2

- Basic ECL Switch
- Required Input Signal
- Transition Region
- Emitter-Follower Buffers
- Multiple Inputs
- Power Conservation, Complementary Functions
- Series Gating, Wired AND
- The Current Source, Output Regulation
- Threshold Regulation
- Temperature Compensation
- Noise Margins
- Mixing F10K and Conventional 10,000 Series Circuits

ECL CIRCUIT BASICS

INTRODUCTION

ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental subcircuits of a simple element. System variables such as supply voltage tolerances and temperature have predictable effects on circuit parameters, thus allowing a systematic evaluation of noise margins. A discussion of mixing F10K and conventional 10,000 circuits emphasizes their compatibility.

BASIC ECL SWITCH

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch *(Figure 2-1),* a logic operation consists of steering the current through either of two return paths to V_{CC}; the state of the switch can be detected from the resultant voltage drop across R1 or R2. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

REQUIRED INPUT SIGNAL

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between Q1 and Q2, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through Q1. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through Q2. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB}. The signal swing is made larger (approximately 850 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another.

TRANSITION REGION

If the voltage at the collector of Q1 is monitored while varying V_{IN} above and below the value of V_{BB}, the relationship between V_{C1} and V_{IN} appears as shown in *Figure 2-2.* Note that the horizontal axis of the graph is centered on V_{BB}; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

EMITTER-FOLLOWER BUFFERS

In *Figure 2-2,* V_{C1} ranges from V_{CC} (gnd) when Q1 is off to approximately –0.98 V when Q1 is conducting all of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch *(Figure 2-3).* In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7 Ω), ECL circuits can drive transmission lines — coaxial cables, twisted pair, and etched circuit — having characteristic impedances of 50 Ω or less.

In this buffered current switch, the collectors of Q3 and Q4 return to a separate V_{CC} lead. This separation insures that any changes in load currents during switching do not cause a change in V_{CC2} through the small but finite inductance of the V_{CC1} bond wire and package lead. Outside the package, the two V_{CC} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is

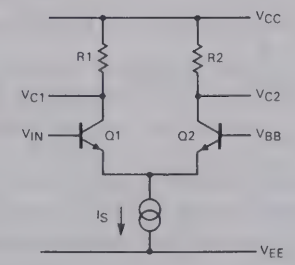

Fig. 2-1. Basic ECL Switch

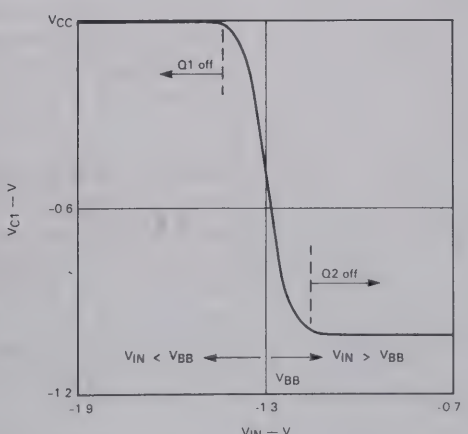

Fig. 2-2. V_{C1} - V_{IN} Transition Region

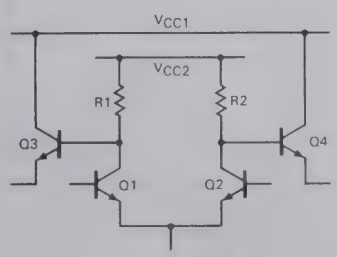

Fig. 2-3. Buffered Current Switch

loaded with 50 Ω returned to –2 V. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data bussing.

MULTIPLE INPUTS

The buffered switch of *Figure 2-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 2-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following suit. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic One signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 2-4* are the bleeder resistors, nominally 50 kΩ, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the buildup of charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the bleeder resistors eliminate the need for external wiring to hold them LOW.

POWER CONSERVATION, COMPLEMENTARY FUNCTIONS

Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in Chapter 6. In the basic switch *(Figure 2-1)*, power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or a transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since many of the ECL elements have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

SERIES GATING, WIRED AND

Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figure 2-5* and *2-6*.

In *Figure 2-5,* if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 2-6,* another pair of transistors is added to obtain the Exclusive OR and Exclusive NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree *(Figure 2-7)*. If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique combina-

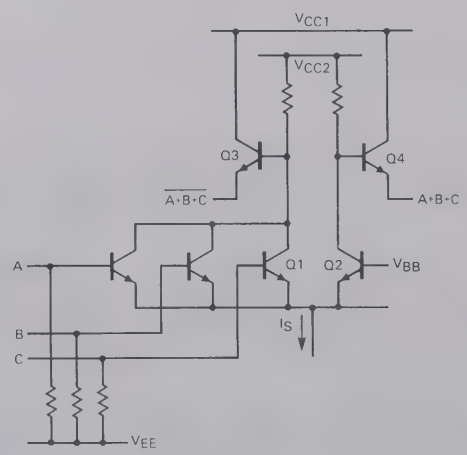

Fig. 2-4. Input Expansion by Parallel Transistors

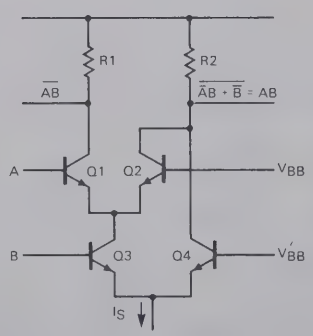

Fig. 2-5. Series/Parallel Gating

tion of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches,with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

THE CURRENT SOURCE, OUTPUT REGULATION

All elements of the F10K and F95K series use a transistor current source illustrated in *Figure 2-8.* Source current is determined by an internally generated reference voltage V_{CS}, the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE}, which makes I_S independent of supply voltage.

Regulating the current source simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α, the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1 V change in V_{EE} changes the output level V_{OL} by only 20 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE}, switching parameters are directly affected. This sensitivity is eliminated in F10K and F95K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE}. By holding I_S constant with V_{EE}, incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE}, causing switch dissipation to change more rapidly with V_{EE}.

In the F10K circuits, the output voltage levels go more positive as temperature increases. Change rates for V_{OH} and V_{OL} are approximately 1.5 and 0.7 mV/°C, respectively. In F95K circuits, output voltage levels are regulated with temperature, discussed later under temperature compensation.

THRESHOLD REGULATION

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB}. In F10K and F95K elements, the on-chip bias driver holds V_{BB} constant with respect to V_{CC}, thus minimizing changes in input thresholds with V_{EE}. For a V_{EE} change of 1 V, for example, V_{BB} changes by approximately 10 mV.

With output voltage levels and input thresholds regulated, F10K and F95K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with –4.7 V and a receiving circuit operated with –5.7 V experience a LOW state noise margin loss of only 15 to 20 mV, compared to the ideal case of both circuits with V_{EE} = –5.2 V. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

In F10K circuits, V_{BB} goes more positive, at a rate of approximately 1.1 mV/°C, as temperature increases. Since the transition region is centered on V_{BB}, the input thresholds change with temperature at the same rate.

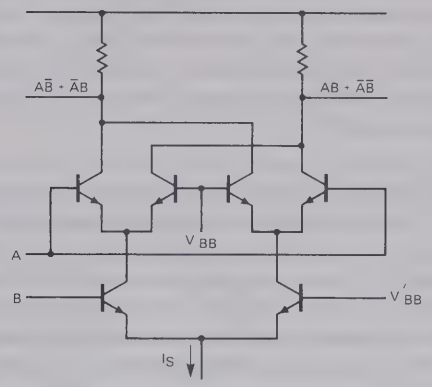

Fig. 2-6. Exclusive OR/NOR

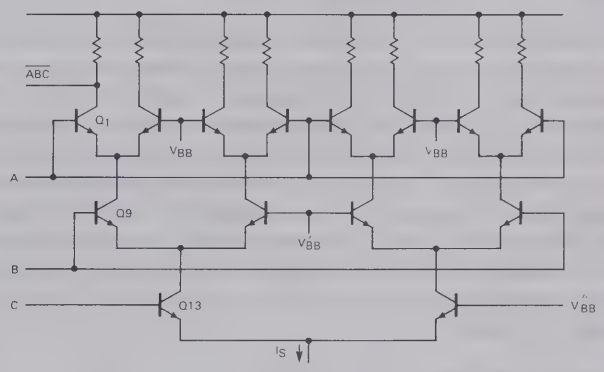

Fig. 2-7. Octal Decoding Tree

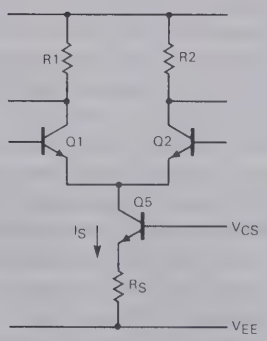

Fig. 2-8. Constant Current Source for a Switch

TEMPERATURE COMPENSATION

The output levels and input thresholds of F10K circuits vary with temperature as do those of conventional 10,000 series circuits. In F95K circuits, input thresholds are made insensitive to temperature by regulating V_{BB}. Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in *Figure 2-9*.[1-5]

With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop across R1 of sufficient magnitude to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately 1.5 mV/°C, while the voltage drop across D1 decreases at the same rate. This means that there is a net voltage increase of 3 mV/°C across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by 1.5 mV/°C, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F95K change rates for V_{OH}, V_{BB}, and V_{OL} are approximately 0.06, 0.08 and 0.1 mV/°C, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, nor do temperature differences cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

NOISE MARGINS

The most conservative values of ECL noise margins are based on the dc test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in *Figure 2-10*, with the boundaries of the input threshold region also identified. The HIGH state noise margin is usually defined as the difference between V_{OHB} and V_{IHB}, with the LOW state margin defined as the difference between V_{OLA} and V_{ILA}. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in *Figure 2-11*. The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of –1.29 V for F10K (at +25°C) or –1.32 V for F95K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB}, which amount to ±60 mV and ±40 mV for F10K and F95K circuits respectively. Using F10K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of –1.23 V, and the input test voltage V_{IHB} is –1.105 V, for a net difference of 125 mV. Similarly, the dashed curve on the left applies when V_{BB} is –1.35 V, with V_{ILA} specified as –1.475, which also gives a net difference of 125 mV. The points V_{IHB}, V_{OHC} and V_{ILA}, V_{OLC} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way V_{IHB} and V_{ILA} are defined. From the transfer function of *Figure 2-11*, for example, V_{IHB} is defined as a value of input voltage which causes a worst case output to decrease from V_{OHB} to V_{OHC}. This change in V_{OH} amounts to only 20 mV for F10K circuits or 10 mV for F95K circuits. Thus, if a worst case OR gate has a quiescent input of V_{OHB}, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 or 20 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc.) with sufficient amplitude to reach the V_{BB} level.

The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short of or exceeds V_{BB}, the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ±50 mV on either side of V_{BB}, a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to its V_{BB}, the output voltage is also equal to V_{BB}, within perhaps 30 mV.

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 2-12*. The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is –5.2 V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F10K circuits at +25°C are used. With typical circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of –1.29 V and V_{OL} of –1.75 V, or 460 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.

Non-typical V_{BB} of gate B. Specifications provide for V_{BB} variations of ±60 mV. If the V_{BB} of gate B is 60 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$$\Delta V_{PL} = -60\ mV$$
$$V_{PL} = 460 - 60 = 400\ mV$$

Non-typical V_{OL} of gate A. V_{OL} limits are –1.65 to –1.85 V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of –1.68 V or lower. Since this value differs from the nominal V_{OL} by 70 mV, V_{PL} must be reduced accordingly.

$$\Delta V_{PL} = -70\ mV$$
$$V_{PL} = 400 - 70 = 330\ mV$$

Difference in ground (V_{CC}) potential between gates A and B. Since the V_{CC} lead of gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of gate A more positive. Minimizing ground drops is one of the system designer's tasks (Chapter 6) and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$$\Delta V_{PL} = -30\ mV$$
$$V_{PL} = 330 - 30 = 300\ mV$$

Difference in V_{EE} between gates A and B. In the polarity shown, V_3 reduces the supply voltage for gate A since it is assumed that gate B has V_{EE} of -5.2 V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1 V change in V_{EE} causes a V_{OL} change of 20 to 30 mV, or 2% to 3%. Assuming a value of 0.5 V for V_3 and adding the 30 mV of V_1, the net reduction in supply voltage for gate A is 0.53 V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$$\Delta V_{PL} = -16\ mV$$
$$V_{PL} = 300 - 16 = 284\ mV$$

If the net supply voltage of gate A is assumed to be -5.2 V, then V_1 and V_3 cause gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of gate B to go more negative at the rate of 10 mV/V of V_{EE} change, or 1%. Thus, for the same values of V_1 and V_3, the required reduction of V_{PL} is only 5 mV instead of the 16 mV computed above. However, if gate A is a conventional 10,000 series circuit, the rate of change of V_{OL} with V_{EE} is much greater, amounting to approximately 25%. Thus, it may not be feasible to allow V_3 to be as great as 0.5 V since the noise margin loss of 125 mV could be prohibitive. It is common practice with these types of circuits to limit V_{EE} differences to about 0.1 V, thus limiting noise margin loss to 25 mV.

Non-typical V_{BB} of gate B. This was considered earlier for its effect at the input of gate B. It must also be considered for its effect on the excursion of the output voltage of gate B. Since the net input voltage of gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of gate B could be 90 mV more negative than the nominal V_{BB} of gate C. This excess excursion must be divided by the voltage gain of gate B to determine exactly how much V_{PL} must be reduced as compensation.

$$\Delta V_{PL} = -90/5.5 = -16\ mV$$
$$V_{PL} = 284 - 16 = 268\ mV$$

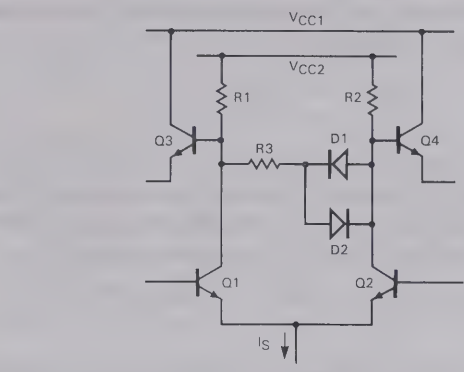

Fig. 2-9. Temperature Compensation

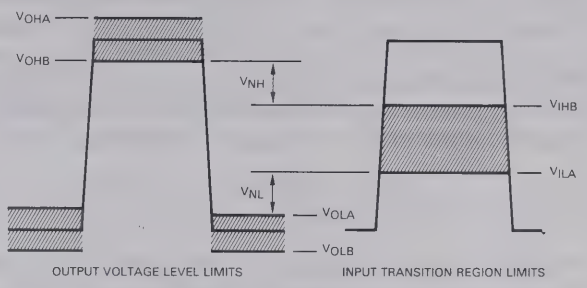

Fig. 2-10. Identifying Specification Limits on Input and Output Voltage Levels

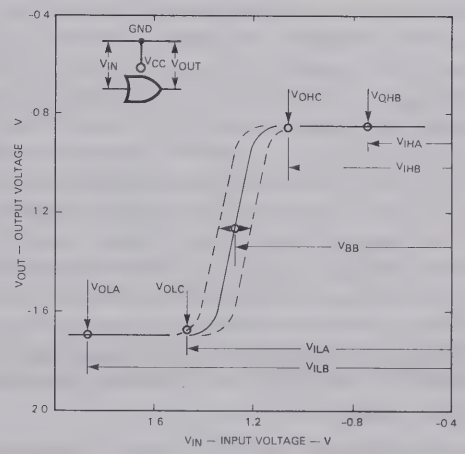

Fig. 2-11. Location of Test Points and Threshold on a Transfer Function

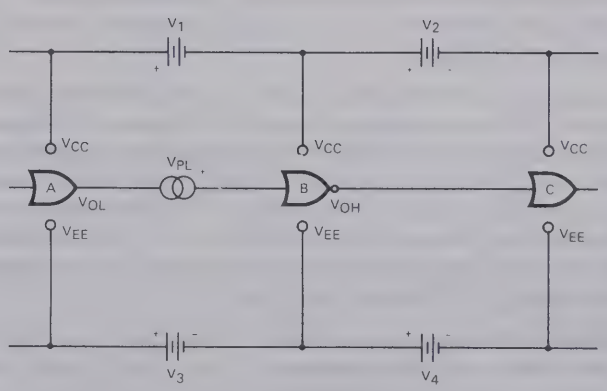

Fig. 2-12. Arrangement for Noise Propagation Analysis

Non-typical V_{BB} of gate C. The V_{BB} of gate C could be 60 mV more positive than the nominal value of −1.29 V. Dividing by the voltage gain of gate B gives the necessary reduction of V_{PL}.

$$\Delta V_{PL} = -60/5.5 = -11 \text{ mV}$$
$$V_{PL} = 268 - 11 = 257 \text{ mV}$$

Difference in V_{CC} potential between gates B and C. For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC} lead of gate C. Assume 30 mV for V_2 as was done for V_1.

$$\Delta V_{PL} = -30/5.5 = -5.0 \text{ mV}$$
$$V_{PL} = 257 - 5 = 252 \text{ mV}$$

Difference in V_{EE} between gates B and C. In the polarity shown, V_4 reduces the supply voltage for gate C, as does V_2. As previously mentioned, V_{BB} changes with V_{EE} at a rate of 10 mV/V, or 1%. Assuming a value of 0.5 V for V_4, as was done for V_2, adding V_2 gives a net V_{EE} reduction of 0.53 V. This makes the V_{BB} of gate C about 5 mV more positive, with respect to its own V_{CC} lead. This must also be divided by the gain of gate B to determine the effect on the permissible value of V_{PL}.

$$\Delta V_{PL} = -5.3/5.5 \simeq -1.0 \text{ mV}$$
$$V_{PL} = 252 - 1 = 251 \text{ mV}$$

If gate C is a conventional 10,000 series circuit, the V_{BB} shift with V_{EE} amounts to approximately 15%, requiring a proportionally larger reduction of V_{PL}.

At this point the more conservatively defined V_{NL} *(Figure 2-10)* should be evaluated and compared with V_{PL}. Subtracting the 25°C values of V_{OLA} and V_{ILA}, a value of 175 mV for V_{NL} is obtained. This automatically accounts for non-typical V_{OL} of gate A and V_{BB} of gate B but does not take into account V_1 and V_3. For the same assumed values of V_1 and V_3, V_{NL} must be reduced by 46 mV, giving a net value of 129 mV. Because of the way it is defined, V_{NL} is not affected by V_2, V_4 or a non-typical V_{BB} of gate C. V_{NL} is defined as the value of noise superimposed on the input of gate B that causes its output to exhibit an excursion to V_{OHC}, which is only 20 mV below the worst case quiescent output level V_{OHB}. This leaves room for negative-going noise to be induced at the input of gate C at the same time V_{NL} is present at the input to B.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the differences in V_{CC} and V_{EE} potentials decrease the noise margins and therefore should be minimized.

Differences in ambient temperature can also decrease noise margins. Referring again to *Figure 2-12,* if gate B is operating at +25°C but the ambient temperature of gate A goes up, then the V_{OL} of gate A goes more positive and thus reduces the noise margin at the input to gate B. The temperature coefficient of V_{OL} is approximately 0.7 mV/°C. If, for example, gate A is operating at +55°C, the noise margin is reduced by the product (0.7) (30) which is 21 mV.

Similarly, if the temperature of gate C increases, V_{BB} of gate C goes more positive at the rate of 1.1 mV/°C. If gate C is operating at +55°C, the allowable noise disturbance is reduced by 33 mV, whether the disturbance is caused by the gate B output excursion or by an independent noise source.

If the temperature gradients are reversed, *i.e.,* if gates A and C remain at +25°C but the temperature of gate B increases, there is an increase in LOW state noise margin at the input of B, because V_{BB} of B is more positive, and an increase in HIGH state noise margin at the input of C because the V_{OH} of B is more positive. The disadvantage comes when gate A changes to the V_{OH} state. In this state, the elevated V_{BB} of gate B subtracts from the HIGH state noise margin at its input. Simultaneously the elevated V_{OL} out of B decreases the LOW state noise margin at the input of gate C. It is apparent that any temperature gradient is a disadvantage because it decreases either the LOW or HIGH state noise margin. This points out the advantage of the F95K series circuits, with output levels and input thresholds only slightly affected by temperature. Data sheet test limits and conditions of F95K circuits automatically include an assumed temperature gradient of ±75°C between communicating circuits. If system temperature conditions are subject to wide variations, the use of F95K circuits is recommended.

MIXING F10K AND CONVENTIONAL 10,000 SERIES CIRCUITS

The F10K series is designed to be fully compatible with 10,000 series elements of other manufacturers. They have the same functions, pinouts, specifications, part numbers and temperature behavior. The F10K series circuits, however, tolerate a much broader range of V_{EE} gradients, regulation, and ripple without degradation of the dc and ac characteristics. If a system is designed to operate with both types of circuits, the more restrictive V_{EE} requirements of conventional 10,000 series circuits must be met.

When the two types of circuits are randomly mixed in the same system, the effects of V_{EE} variations and gradients on noise margins are not identical for all combinations of driving and receiving circuits. In the general case of two communicating circuits such as gates A and B in the arrangement for noise propagation analysis *(Figure 2-12),* there are four possible combinations of circuit types; the driver can be either an F10K or a 10,000 series and so can the receiver. If gate A is in the V_{OL} state and both gates start with a V_{EE} of −5.2 V, the LOW state noise margin decreases if the V_{EE} of gate A goes more positive, because the V_{OL} goes more positive. The V_{OL} shift is only 2% of the V_{EE} change if gate A is an F10K type, but the shift is 25% of the V_{EE} change if gate A is a conventional 10,000 series type. If the V_{EE} of gate A is held at −5.2 V and the V_{EE} of gate B goes more negative, the LOW state noise margin decreases because the V_{BB} of gate B goes more negative. This in turn, shifts the entire transition region more negative. The shift is only 1% of the V_{EE} change if gate B is an F10K type, but is 15% of the V_{EE} change if gate B is a conventional 10,000 series type. If the two supply voltages vary independently about −5.2 V, then the effects of the V_{OL} shift of gate A and the V_{BB} shift of gate B are additive, which gives the worst case loss of noise margin.

If gate A is in the V_{OH} state, its output is not affected by V_{EE} changes, assuming that the input of A is not biased in the transition region. If the V_{EE} of gate B goes more positive, the HIGH state noise margin is reduced by the positive going shift of the V_{BB} of gate B. Again, the shift is 1% of the V_{EE} change if B is an F10K circuit or 15% of the V_{EE} change if B is a conventional 10,000 series type.

In large systems designed with the conventional 10,000 series circuits, it is common practice to restrict V_{EE} tolerance to ±2% and V_{EE} gradients to 2% or less between circuits communicating in the single-ended mode. This keeps noise

margin losses to manageable levels, considering that differences in temperature and V_{CC} potential must also be accommodated.

The noise margin between two circuits as a function of V_{EE} gradients is shown in *Figure 2-13* for the four possible combinations of circuit types. The margins shown are either V_{NH} or V_{NL}, whichever is least. This is in recognition of the fact that noise can be of either polarity and thus the smaller of V_{NH} or V_{NL} is the critical margin for the system. The graph assumes that both the driving and receiving circuit start with the nominal V_{EE} of –5.2 V and then the V_{EE} shifts by the same magnitude but in opposite directions at the two circuits. The horizontal axis of the graph indicates the net difference in V_{EE} between the two circuits. The mixed combinations B and C either have the same or improved noise margins compared to the conventional 10,000 series types (combination A), while the F10K combination is only slightly affected by gradients. Differences in temperature and V_{CC} potential are not considered in this graph, but they have the same effects with either type of circuit.

When V_{EE} changes in the same direction at both the driving and receiving circuit, *i.e.,* no gradient, the worst case losses of noise margin are less than in the case of a gradient. *Figure 2-14* shows noise margin as a function of $\pm V_{EE}$ tolerance. Again, the noise margins shown are the smaller of V_{NH} or V_{NL}, and differences in temperature and V_{CC} potential are not considered.

REFERENCES

1. Marley, R.R., "On-Chip Temperature Compensation for ECL", Electronic Products, (March 1, 1971).
2. Marley, R.R., "Design Considerations of Temperature Compensated ECL", IEEE International Convention, (March, 1971).
3. Muller, H.H., Owens, W.K., Verhofstadt, P.W.J., "Fully Compensated ECL", ISSCC Digest of Technical Papers, (February, 1973).
4. Widlar, R.J., "New Developments in IC Voltage Regulators", ISSCC Digest of Technical Papers, (February, 1970).
5. Widlar, R.J., "Local IC Regulator For Logic Circuits", Computer Design, (May, 1971).

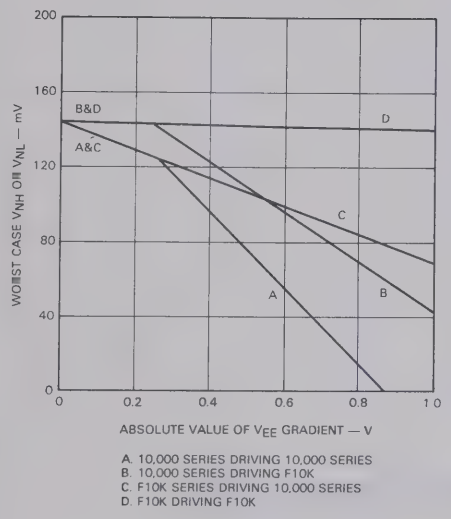

Fig. 2-13. Worst Case Noise Margin Versus V_{EE} Gradient

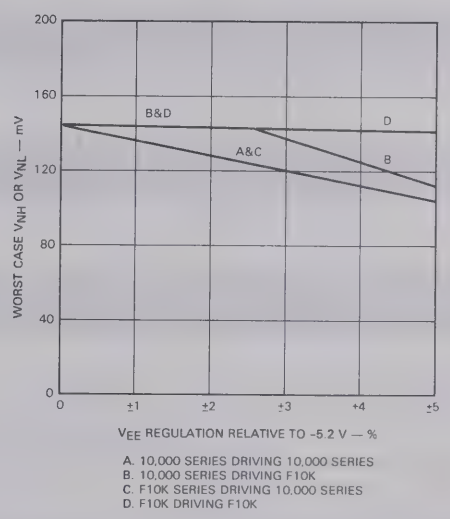

Fig. 2-14. Worst Case Noise Margin Versus V_{EE} Tolerance

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CHAPTER 3

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- MSI
- Counters
- Shift Registers
- Multiplexers
- Decoders/Demultiplexers
- Comparators
- Parity Generation and Checking
- Converting a TTL Design to ECL

ECL LOGIC DESIGN

INTRODUCTION

The 10K and 95K ECL families offer a broad line of SSI, MSI and memory functions. Basic gates and flip-flops are described, followed by design applications using ECL MSI. Finally, a few guidelines are given to help designers, already familiar with DTL and TTL, to readily convert to ECL.

Fairchild ECL logic symbols use the positive logic or "active level HIGH" option of MIL-STD-806B. Logic One is therefore by definition the most positive algebraic voltage, *i.e.,* nearest ground. Logic Zero is the most negative, nearest V_{EE}. In some cases it may be easier to think in terms of negative logic; for example, a positive logic OR is a negative logic AND. The positive and negative logic symbols for the common gating types are shown in *Figure 3-1.*

OR/NOR GATES

The most basic ECL circuit is the OR/NOR gate *(Figure 3-2).* If the input voltages are more negative than the reference voltage V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 low. If either input is more positive than V_{BB}, Q1 or Q2 conducts and Q3 is cut off, raising its collector voltage. Because one or more transistors always conduct, there is a constant current drain, independent of frequency, that eliminates sharp switching transients and frequency dependent power dissipation effects.

Outputs of the circuit, emitter followers Q4 and Q5, provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. Because of the differential nature of the input circuit, the V_{EE} supply sees a constant current load, which minimizes noise on the supply line. A single circuit, shown as a block at the base of Q3 in *Figure 3-2,* is used to generate the reference voltages for all gates on the chip.

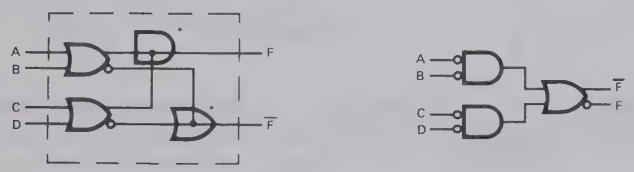
Since the basic gate simultaneously performs the positive logic OR and NOR functions, both True and Complement outputs are provided within the same delay period of a single

POSITIVE LOGIC NEGATIVE LOGIC TRUTH TABLE

OR/NOR

A	B	F	$\bar{F}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

OR/AND, OR/AND/INVERT



*INTERNAL SERIES CONNECTION, NOT THE WIRED-OR

A	B	C	D	F	$\bar{F}$
L	L	X	X	L	H
X	X	L	L	L	H
H	X	H	X	H	L
H	X	X	H	H	L
X	H	H	X	H	L
X	H	X	H	H	L

EXCLUSIVE OR/NOR

A	B	F	$\bar{F}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = Most Positive Voltage — HIGH
L = Most Negative Voltage — LOW
X = Don't Care

Fig. 3-1. Positive and Negative Logic Symbols for Common ECL Gates

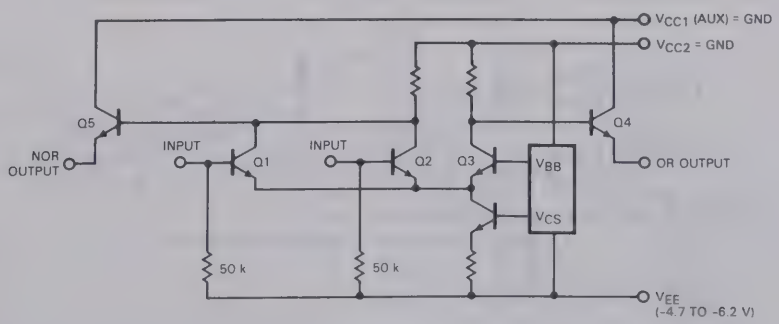


Fig. 3-2. Basic ECL Gate

gate. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor is necessary in all cases.

Variations among ECL OR/NOR gates are the number of gate inputs, the common inputs, and the output polarities. Note from *Figure 3-1* that AND or NAND function can be obtained by complementing the inputs. When OR gate outputs are wired-OR, the effect is to widen the OR gate *(Figure 3-3)*. This wired-OR is a True, positive logic wired-OR and should not be confused with a DTL positive logic wired-AND or internal series gating used for some ECL functions.

OR/AND, OR/AND/INVERT GATES

These gates utilize internal series AND gating to achieve a second gating level as described in Chapter 2. Note that this connection is internal to the device and cannot be modified by external connection *(Figure 3-4)*. The AND gating is obtained with minimum propagation delay and noise immunity penalty.

FLIP-FLOPS

ECL flip-flops are similar to conventional TTL flip-flops but there are fewer types available. *Figure 3-5* illustrates two workhorses — the 95029, a $\overline{JK}$ flip-flop with multiple $\overline{J}$,$\overline{K}$, and clock gating, and the F10131 dual D flip-flop containing two edge triggered master/slave flip-flops. Many gate functions are achieved internally without incurring a full gate delay. In the 95029, the $\overline{J}$ input is activated when all $\overline{J}$ inputs are LOW (or open); the $\overline{K}$ inputs operate in a similar manner. The three clock inputs allow data to be entered into the master when all clock inputs are LOW and loaded into the slave when any clock input goes HIGH.

The 10131 contains two master/slave, D flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state

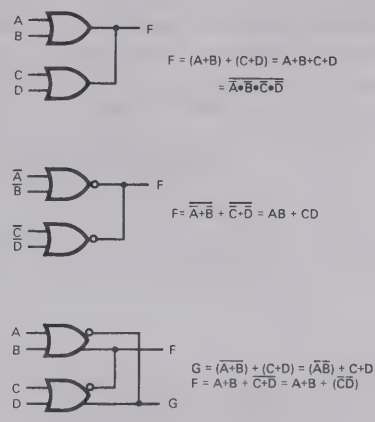


Fig. 3-3. OR/NOR Gates and the Wired-OR Connection

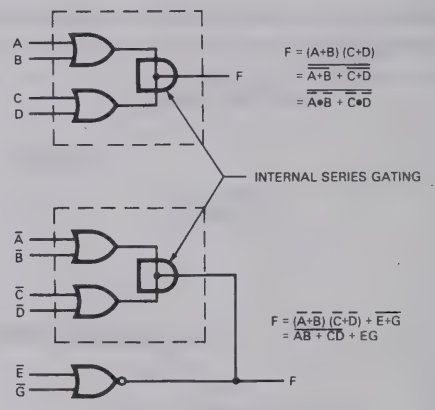
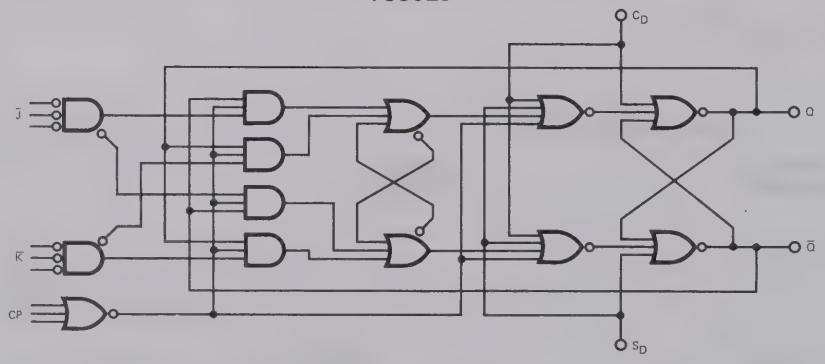


Fig. 3-4. OR/AND Gates and the Wired-OR

F95029



F10131

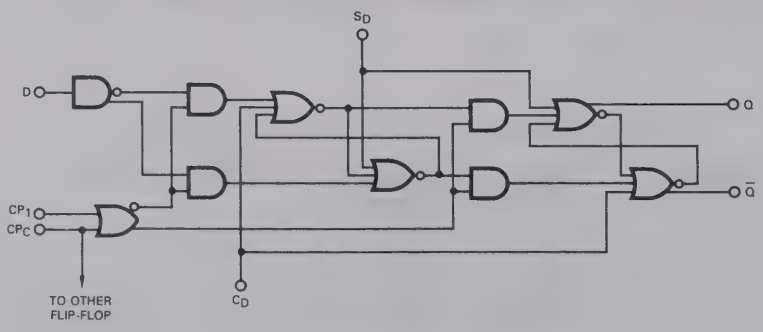


Fig. 3-5. Typical ECL Flip-Flops

making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Both have buffered outputs that can be wired-OR. Output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

When four D flip-flops with common clocks are required, the use of the 10000/95000 shift register, 10010/95010 decade counter or 10016/95016 binary counter should be considered. By holding the $\overline{PE}$ input LOW (or open), the circuits operate as four D flip-flops *(Figure 3-6)*.

MSI

ECL MSI logic is functionally similar to TTL. Designs are sometimes modified for an additional ground connection required for noise reasons and this means one less logic connection. Also, the active levels of the input and output are sometimes changed to optimize OR/NOR gate functions. The similarity of ECL flip-flops and MSI to TTL functions is illustrated in *Figure 3-7* (on the following page).

Counters

The 10010/95010 BCD decade counter and 10016/95016 4-bit binary counter provide the basis for most synchronous counting applications. They are similar in basic configuration and utilize synchronous parallel entry and asynchronous master reset. A Count Enable input and Terminal Count output provide for easy expansion to longer counters.

- Modulo n Counters — Synchronous parallel entry allows the 10016/95016 to divide by any modulo from 2 to 16 as shown in *Figure 3-8*. When the terminal count is reached, the parallel inputs are loaded synchronously. This in turn determines the number of clock pulses required before the $\overline{TC}$ output goes LOW again.

- Expanding the Counters — The 10016/95016 can be expanded by adding flip-flops or more 10016/95016 stages. A divide-by-64 counter is shown in *Figure 3-9* utilizing a 10016 4-bit counter and 10131 dual D flip-flop. Two or more counters can be expanded synchronously as illustrated by the 4-decade counter in *Figure 3-10*. If the 10010

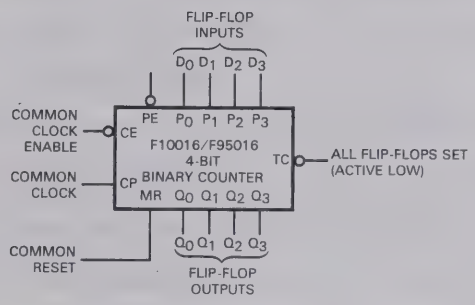


Fig. 3-6. 10016/95016 used as Four D Flip-Flops

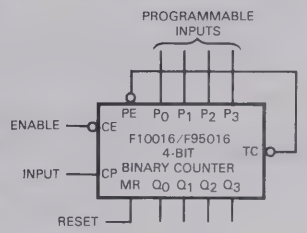


Fig. 3-8. Programmable Divider

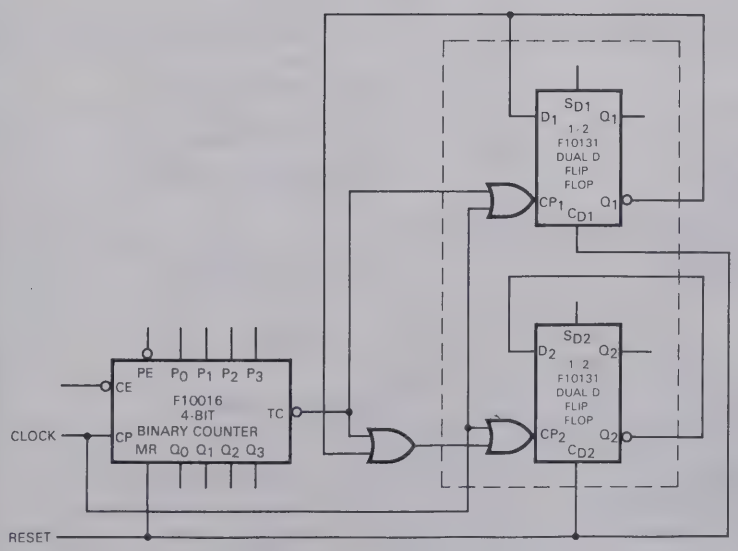


Fig. 3-9. Modulo 64 Counter

DIVIDE RATIO	INPUT REQUIRED			
	P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

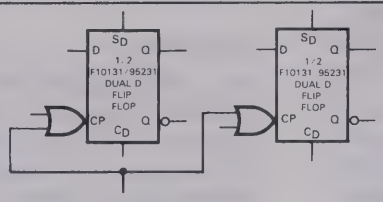
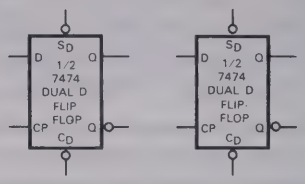
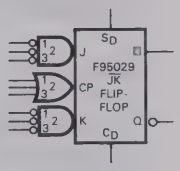
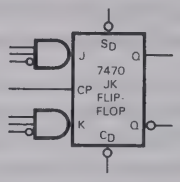
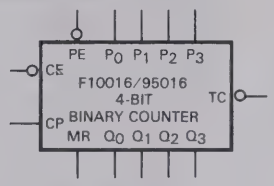
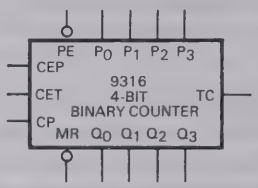
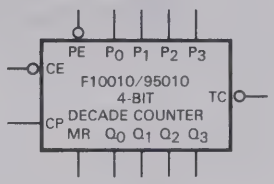
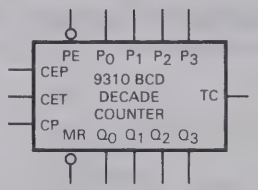
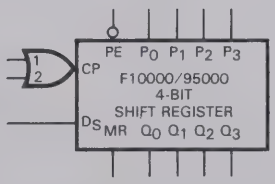
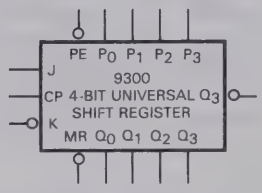
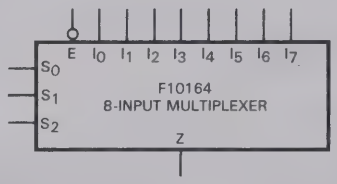
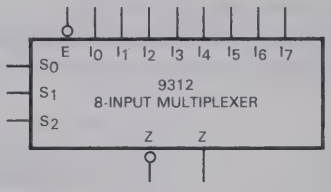
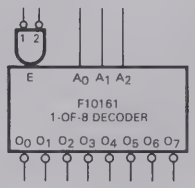
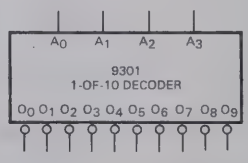
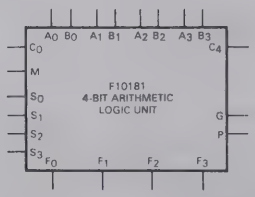
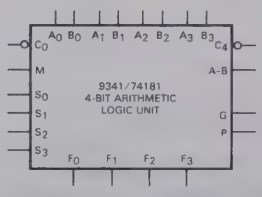
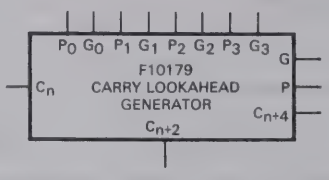
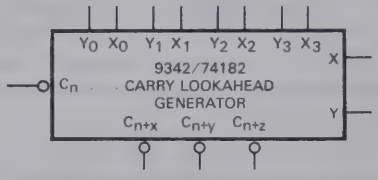
FUNCTION	ECL	TTL
Dual D Flip-Flop		
$\overline{JK}$ Flip-Flop		
4-Bit Binary Counter		
4-Bit Decade Counter		
4-Bit Shift Register		
8-Input Multiplexer		
1-of-8 Decoder		
4-Bit ALU		
Carry Lookahead Generator		

Fig. 3-7. ECL and TTL Function Similarity

is replaced with 10016, the circuit becomes a 16-bit binary counter. An expanded modulo n counter (greater than four bits) can be implemented by using multiple 10016/95016 counters with OR gates driving all CE inputs. The gate inputs are the TC signals of all counters.

- Quasi-Ripple Counters — To reduce gating and slightly increase operating frequency, the scheme of *Figure 3-11* can be used. The $\overline{TC}$ of one stage becomes the clock of another. Care must be taken that output skew does not introduce system hazards; parallel entry cannot be used.

- Modulo 10 Counter with 50% Duty Cycle — A special purpose decade counter with symmetric divide-by-10 output is shown in *Figure 3-12.* The diode resistor combination supplies a logic One; an unused gate can be used for the same purpose.

- Counter Shift Register — The synchronous parallel entry feature allows simple implementation of counters capable of shifting contents serially. The connection is shown in *Figure 3-13;* the $\overline{PE}$ becomes the shift/count (HIGH = count) mode control.

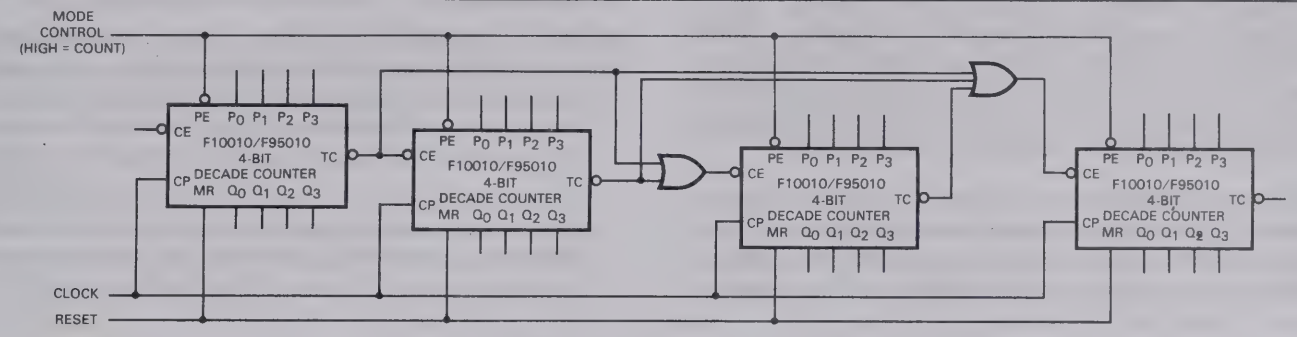


Fig. 3-10. 4-Decade Synchronous Counter

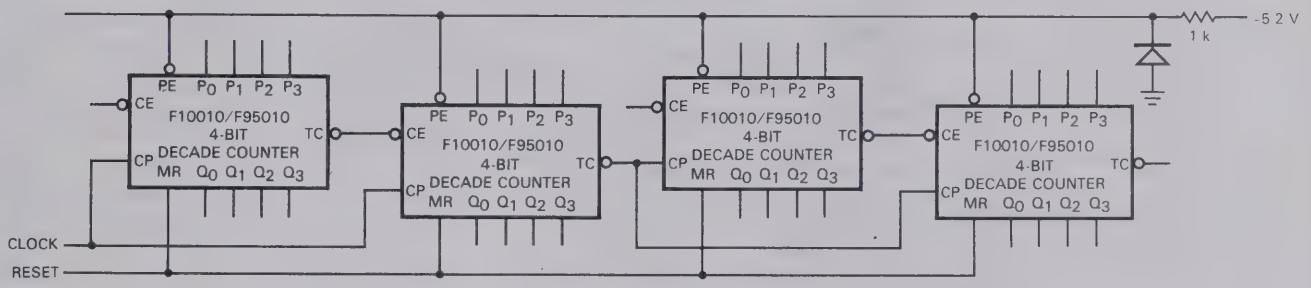
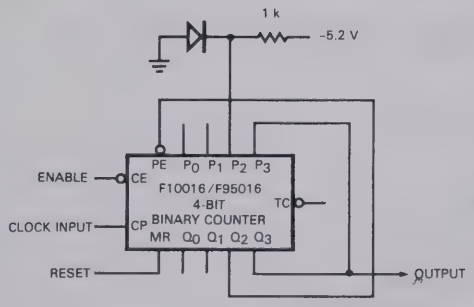


Fig. 3-11. Decade Counter with Ripple Between Decades 2 and 3



COUNT SEQUENCE

Q_0	Q_1	Q_2	Q_3
0	0	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

Fig. 3-12. Modulo 10 Counter with 50% Duty Cycle

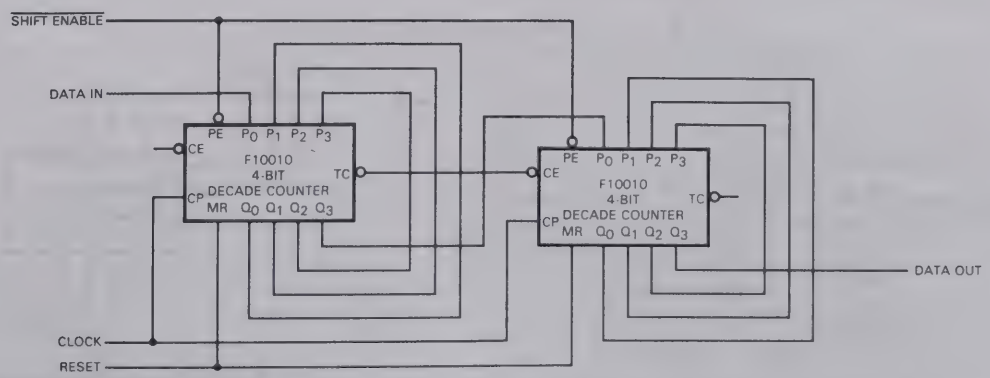


Fig. 3-13. Combination Counter/Serial Shift Register

Shift Registers

The 10000/95000 4-bit shift registers are ideal for most shift register applications.

- Parallel-To-Serial Converter with Control — The circuit of *Figure 3-14* accepts eight bits of parallel data, stores it and shifts it out serially. The addition of 1/2 of a dual flip-flop and 1/2 of a gate package supplies the control function. To analyze the operation, assume the parallel data has been loaded and is being shifted out. The output of the wired-OR (in effect a 7-input AND gate with active LOW inputs and outputs) is HIGH, introducing Ones into the 10131 flip-flop and Zeros into the 10000 shift registers. After seven pulses, the gate output goes LOW and loads new parallel data on the eighth clock, while setting the 10131 to Zero and introducing a timing bit. The entire operation can be controlled by an active LOW clock enable.

- Serial-To-Parallel Converter with Control — The same concept of combining control and data bits to simplify logic can be used for a serial-to-parallel converter. Two 10000/95000 shift registers are connected as a 7-bit serial-to-parallel converter in *Figure 3-15*. To analyze the circuit, assume a Zero has appeared on the data ready line. On the next clock edge, data is entered into Q_0 and a Zero into Q_1 of the left register. All other positions are loaded with Ones. As more clock pulses occur, data is shifted in serially and the data ready line is HIGH until seven data bits are stored. At that point, the data ready line goes LOW, indicating parallel data is ready and the cycle repeats. The separate clock enable is active LOW . Note the use of a resistor and diode to obtain a non-saturating logic HIGH voltage level; this may also be obtained from the output of an unused gate.

- Shift Left/Shift Right Register — The 10000/95000 can be used as a shift left/shift right register by utilizing the parallel inputs to achieve the shift left mode. *Figure 3-16* shows a single 10000 connected in this mode; any length shift register can be obtained by adding more registers.

- Shift Register with Two Inputs — If data is to be received and shifted into a register from one of two sources, the synchronous Parallel Enable can be used to save some gating. *Figure 3-17* shows the connection.

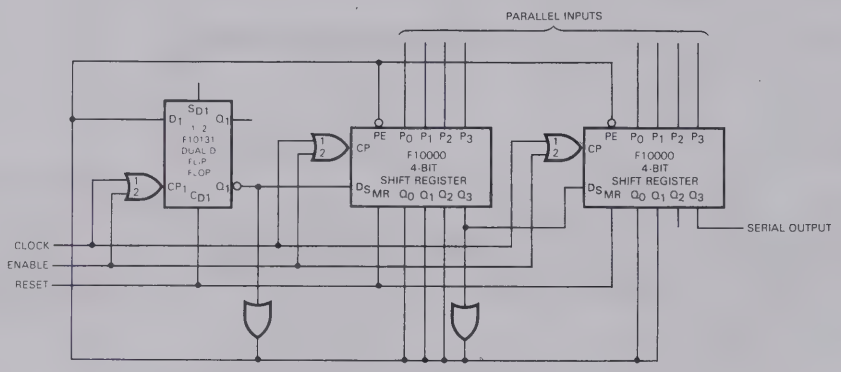


Fig. 3-14. 8-Bit Parallel-to-Serial Converter with Control

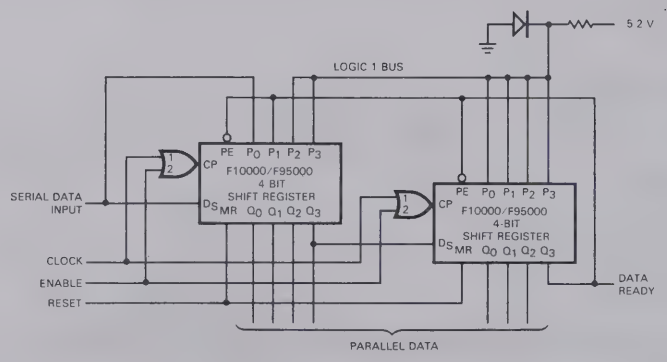


Fig. 3-15. 7-Bit Serial-to-Parallel Converter

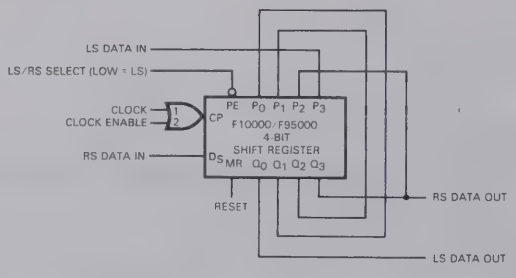


Fig. 3-16. Shift Left/Shift Right Register

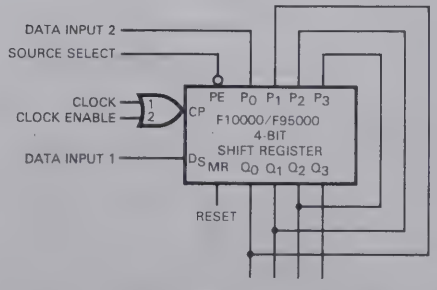


Fig. 3-17. Parallel Enable is used to Select One of Two Serial Inputs

- Shift Register Counters — Shift registers are commonly used to implement a variety of high speed counters as shown in *Figure 3-18.* A ring counter has a single bit different than the rest of the bits and the output is returned to the input. To obtain a modulo n counter, n bits of shift register are used and no decoding is required. A Johnson counter employs feedback from the last stage back to the first such that the input is the opposite state of the output. A modulo n counter requires n/2 shift register stages; any state may be decoded with a 2-input gate. Feedback shift registers use a variety of logic gating to the first stage. An n-stage shift register provides a $2^n - 1$ modulo counter.

  All three shift counter methods require logic to insure against lock-up in unallowed states. More details on shift register counters may be found in the Fairchild TTL Applications Handbook.

Multiplexers

Multiplexers route one of several inputs to a single output. Multiplexer functions can be implemented with standard gates and the wired-OR connection. *Figure 3-19* illustrates a quad-2 input multiplexer implemented with NOR gates. Note that the gates can be physically located in different parts of the system, with lines Z_0 to Z_3 functioning as single-ended data busses, as long as wired-OR connection rules are met. The 10121 OR/AND gate can be used as a 4-input multiplexer as shown in *Figure 3-20.*

The 10164 is an 8-input multiplexer. The 10132 and 10174 are dual multiplexers. The 10173 is a quad 2-input multiplexer. They can be used for a variety of applications.

- Parallel-to-Serial Data Transmission — Two 10164 multiplexers are utilized to convert 16 channels of data to a single twisted pair transmission line *(Figure 3-21).* If the 16 channels carry serial data at 5 MHz, the data is multiplexed and transmitted over a single line at an 80 MHz rate.

- Decade Demultiplexer — A decade demultiplexer controlled by a decade counter is shown in *Figure 3-22.* The Terminal Count output of the 10010 is used to simplify gating.

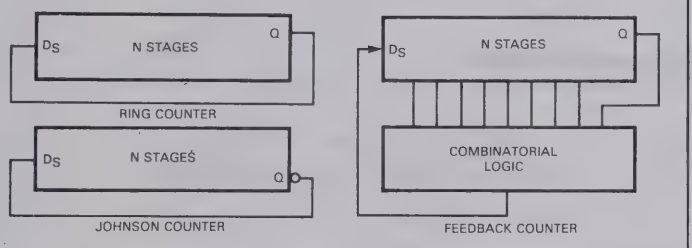


Fig. 3-18. Shift Registers used as Counters

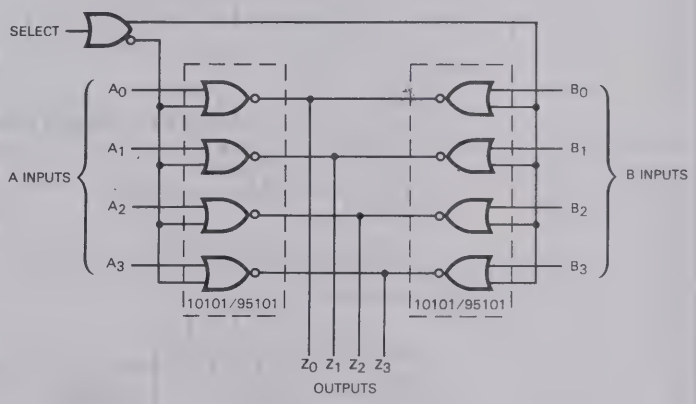


Fig. 3-19. Quad 2-Input Multiplexer using NOR Gates

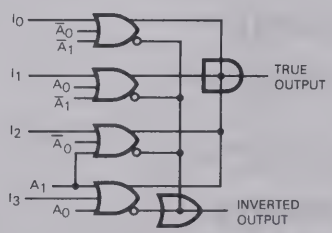


Fig. 3-20. 4-Input Multiplexer using 10121

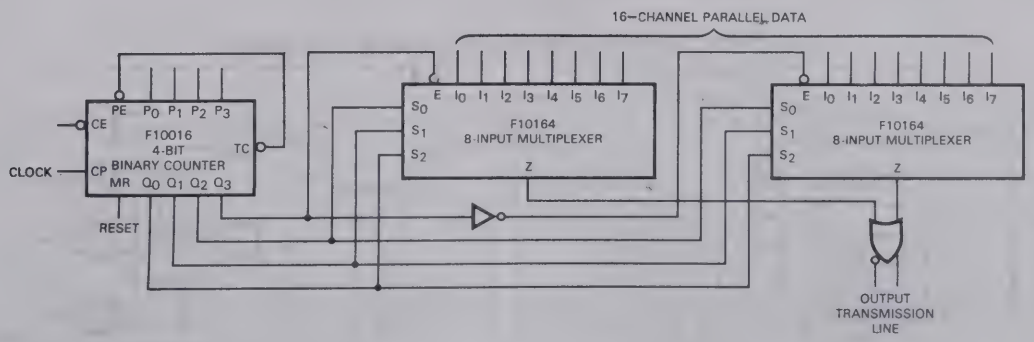


Fig. 3-21. 16-Input Multiplexer

- Digital Function Generator — An 8-input multiplexer can be used to generate any function of four variables without additional logic. This concept is illustrated in *Figure 3-23* with a sample truth table and implementation for a desired 4-variable function F. Three of the variables are connected to the Select inputs while the fourth variable and its complement are connected to various Data inputs. In the example, A is connected to S_2, B to S_1 and C to S_0. Therefore, when A = B = C = 0, the I_0 input of the multiplexer is selected. The truth table indicates that this condition yields a Zero output when D is One or Zero; therefore, I_0 is designated a logic Zero, *i.e.,* open. When ABC = 001, I_1 is selected. From the truth table, the output is a One when D is logic Zero, and a Zero when D is a logic One; therefore I_1 is connected to $\overline{D}$. Connections to the other inputs are determined in the same manner to complete the function. Note the use of a diode-resistor combination to obtain a HIGH logic One input. An unused gate can be used to achieve the same function.

  The function can also be implemented with 1 1/4 gate packages if both True and Complement inputs are available, or with 2 1/4 gate packages if only True inputs are available.

Decoders/Demultiplexers

For decoding or demultiplexing, the True and Complement outputs and the wired-OR feature of the basic gates can be used to make decoders with a single gate delay. For example,

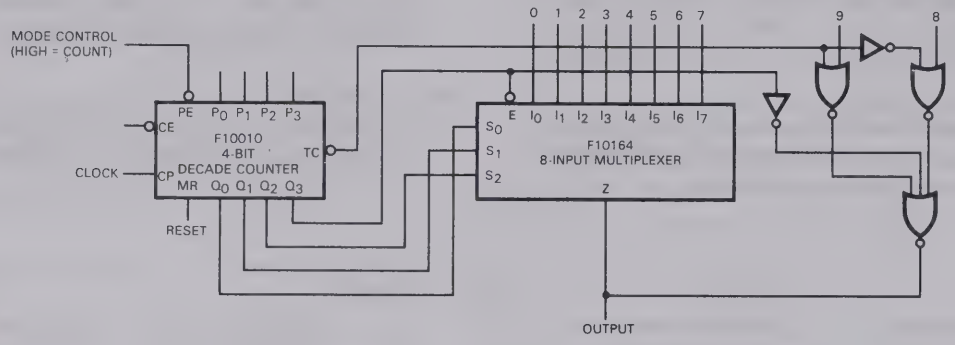
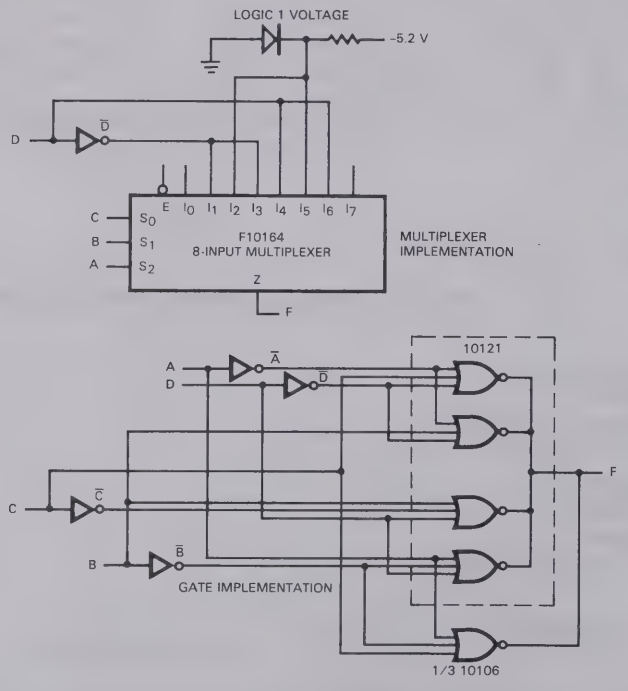


Fig. 3-22. Decade Counter and Demultiplexer



A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

DESIRED FUNCTION $F = A\overline{C}D + A\overline{B}D + \overline{B}C\overline{D} + \overline{A}B\overline{D} + \overline{A}B\overline{C}$

Fig. 3-23. Multiplexer Utilized as a Function Generator

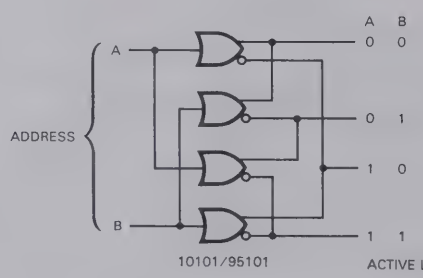


Fig. 3-24. 2 to 4-Line Active Low Decoder

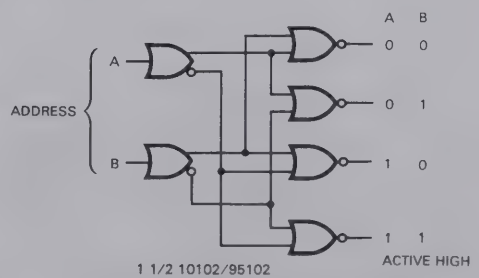
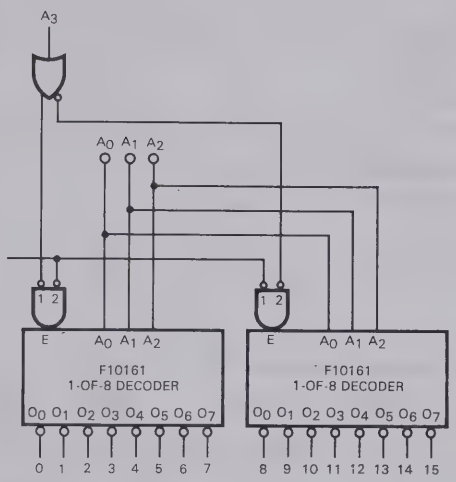


Fig. 3-25. 2 to 4-Line Active High Decoder

Figure 3-24 is a 2 to 4-line, active LOW decoder. If added delay can be tolerated, the 2 to 4-line, active HIGH decoder of *Figure 3-25* can be used.

The 10161 1-of-8 demultiplexer/decoder is designed to decode a 3-bit input word to one of eight active LOW outputs. Two Enable inputs force all outputs HIGH when either Enable input is HIGH. The 10162 1-of-8 demultiplexer/decoder is similar to the 10161 except that the selected output is HIGH; all others are LOW. The 10171 is a dual 1-of-4 demultiplexer/decoder with selected outputs LOW; the 10172 is similar with selected outputs HIGH. These demultiplexer/decoders can be used for a variety of applications.

- 4-Bit Code Decoding — The Enable inputs permit use of two 10161 or 10162 decoders to decode any 4-bit weighted or unweighted code by selecting the appropriate outputs in the required sequence. *Figure 3-26* shows the connection diagram and decode table for this application with active LOW outputs. The function is controlled by the other Enable input; propagation delay is typically 5 ns.
- Decade Decoder — While the universal 4-bit decoder method can be used for 1248 BCD, a more economical approach is shown in *Figure 3-27.* Note that no enable is provided for outputs 8 and 9.
- Memory Decoding — A major decoder application is in address decoding of high speed memory systems. The Enable inputs allow the use of several decoders to decode words of greater than four bits as illustrated in *Figure 3-28.* Four packages are used to select one of 32 active HIGH outputs in 6 to 9 ns from the time of application of the address at inputs A_0 through A_4. This technique can be extended



OUTPUT SELECTION

DECIMAL DIGIT	BCD CODE				
	8421	5421	EXCESS 3	EXCESS 3 GRAY	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Fig. 3-26. Universal 4-Bit Decoder

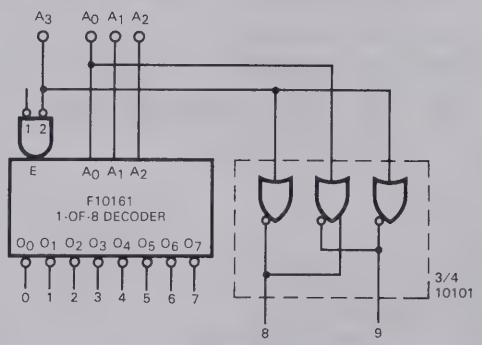


Fig. 3-27. 1248 BCD Decade Decoder

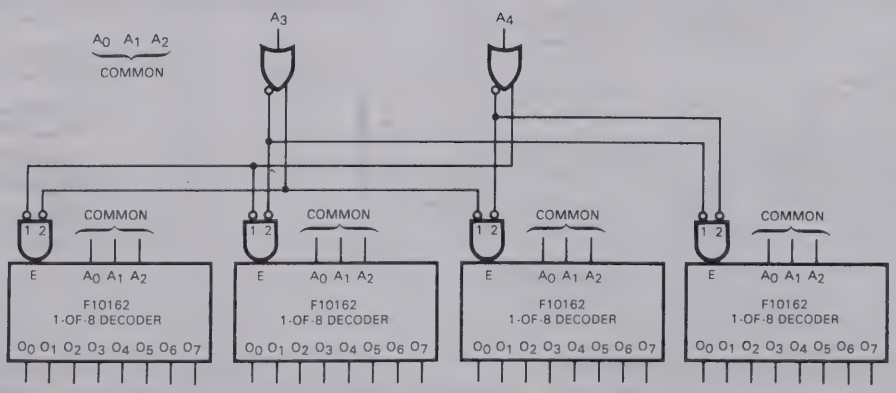


Fig. 3-28. 1-of-32 Active HIGH Decoder

to a 6-bit address by using the LOW output of the 10161 to select one decoder from a group of decoders. *Figure 3-29* shows a 1-of-64 decoding scheme with typical propagation delays of 8 to 12 ns. The remaining Enable input can be used for overall control or wider decoding if desired. 1-of-8 decoders, *e.g.,* the 10161, can be used to demultiplex serial data to parallel outputs by connecting the serial data source to an Enable input *(Figure 3-30).* The other Enable input functions as a data enable line, while inputs A_0, A_1 and A_2 determine which of the eight output lines receives the data. The data is not inverted through the demultiplexer since both the input and outputs are active LOW.

Comparators

A variety of high speed comparators can be defined using ECL gating structures. *Figure 3-31* illustrates a 4-bit identity comparator utilizing two 10121 OR/AND gates.

A 6-bit identity comparator utilizing two 10107 Exclusive OR/NOR gates is shown in *Figure 3-32.* Only True inputs are required and equality is indicated by a LOW on the comparator output.

Parity Generation and Checking

The 10160 typically provides 12-bit parity generation in 3 ns. Its output is HIGH if an odd number of inputs are HIGH.

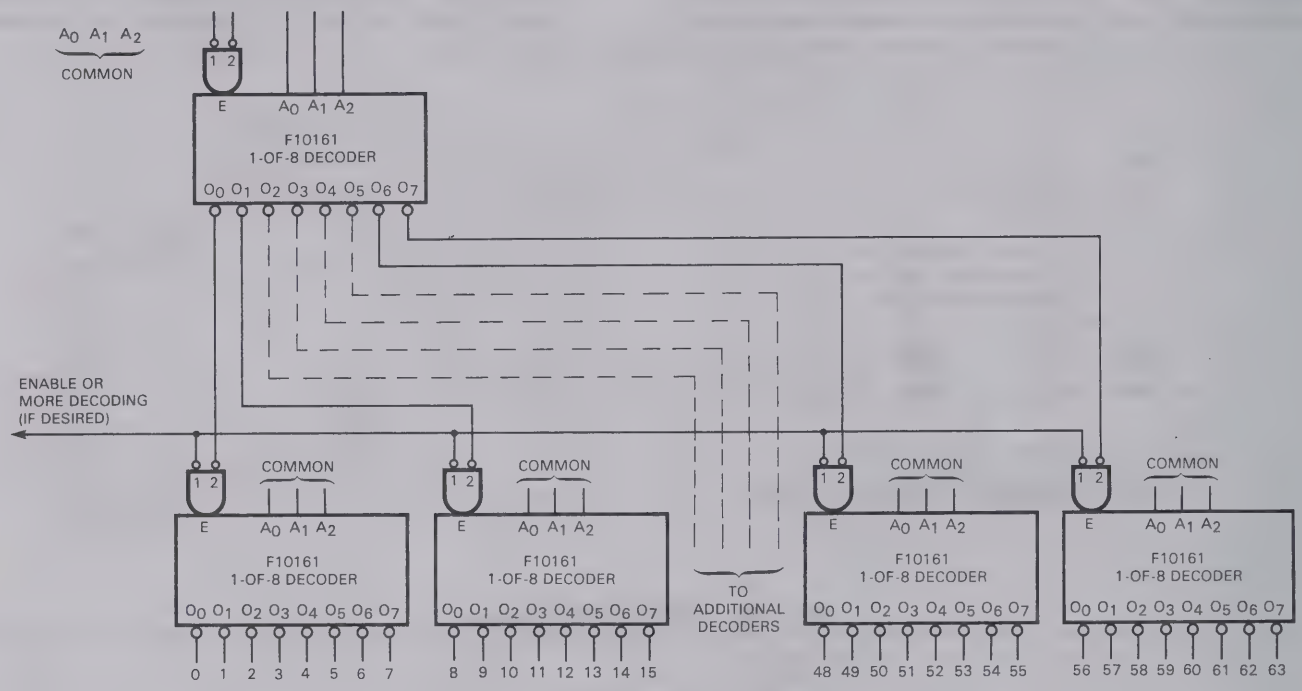


Fig. 3-29. 1-of-64 Active LOW Decoder

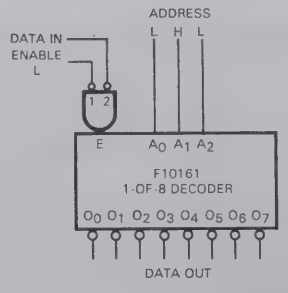


Fig. 3-30. 8-Output Demultiplexer

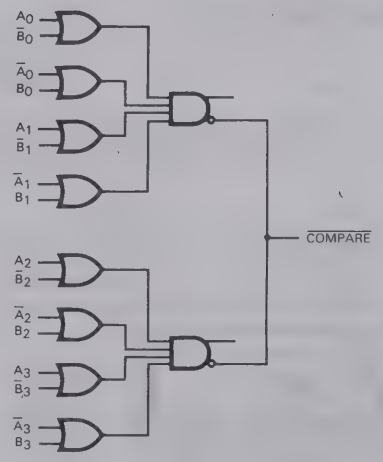


Fig. 3-31. 4-Bit Identity Comparator Using Two 10121 OR/AND Devices

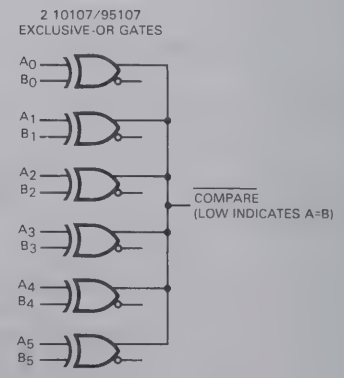


Fig. 3-32. 6-Bit Identity Comparator Requiring True Inputs Only

Figure 3-33 illustrates a 48-bit parity circuit using four 10160s and a 10107 Exclusive-OR gate; typical total delay is 7 ns.

CONVERTING A TTL DESIGN TO ECL

Conversion of TTL design to ECL is straightforward. The NAND gate is the most common TTL logic element, with NOR, OR, and AND gates also available. Clearly, OR and NOR functions are readily available with ECL. The NAND and AND functions are obtained from the ECL OR/NOR function by complementing the inputs as shown in *Figure 3-34a.* NAND gates of five or more inputs are formed by complementing the inputs to ECL OR gates and OR wiring the outputs *(Figure 3-34b).* The AND/OR function is obtained in ECL by using wired-OR NORs *(Figure 3-34c),* the AND/OR/INVERT by using ECL OR/AND gates *(Figure 3-34d).*

From these examples, a simple rule can be determined. To convert from TTL to ECL, complement the ECL gate inputs and use True ECL outputs. However, this approach does not necessarily yield optimum designs because it does not take advantage of the ECL wired-OR capability.

Figure 3-35 illustrates the conversion methods. In *Figure 3-35a,* a TTL circuit converted to ECL requires about 2-1/2 packages assuming no cost for unused functions. In other

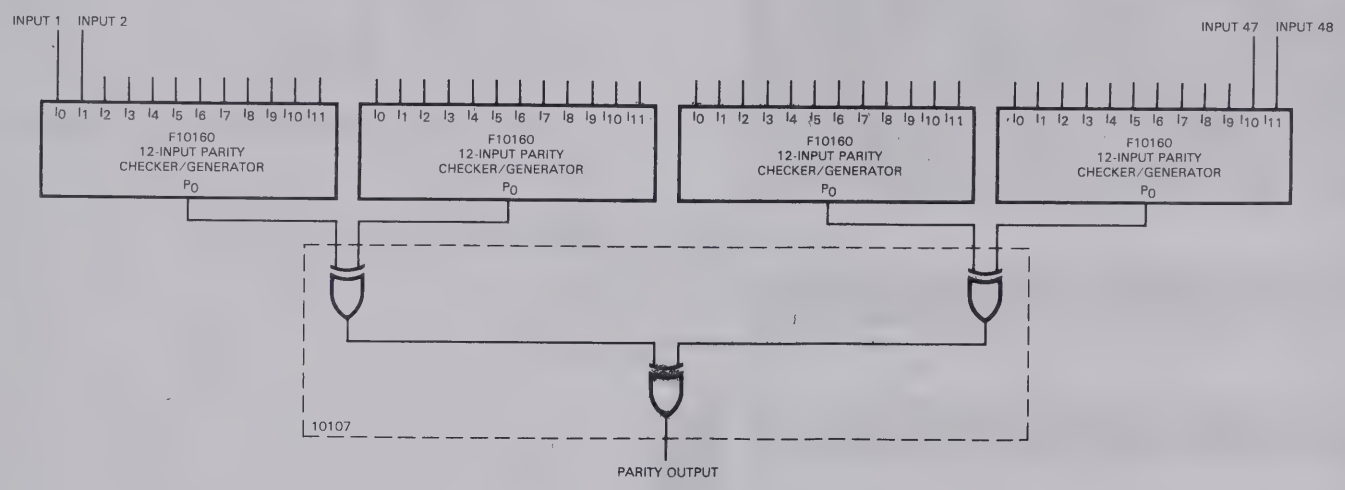
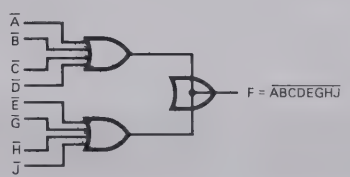
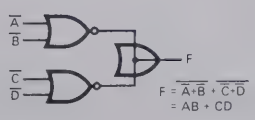


Fig. 3-33. 48-Bit Parity Checker/Generator with Typical Delay of 10 ns

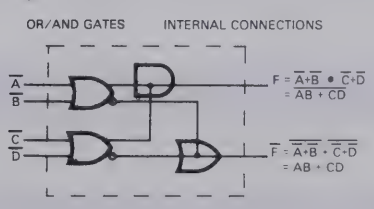
a. NAND Function Obtained by Complementing Inputs



b. Wide NAND Gates Obtained by Using Complemented Inputs and Wired-OR



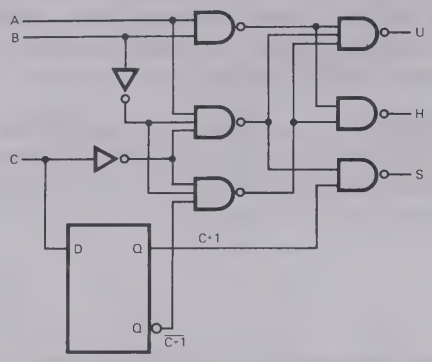
c. NOR Gates Perform AND/OR Function



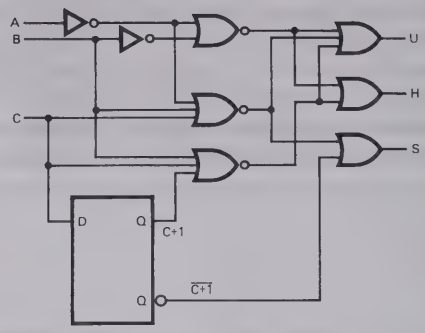
d. OR/AND Gates Perform AND/OR/INVERT Function

Fig. 3-34. Common ECL Logic Functions

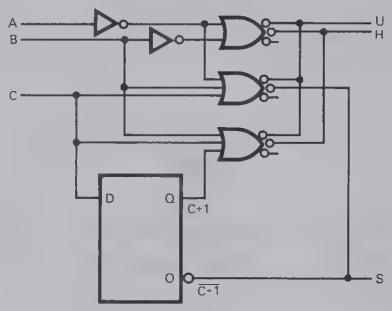
words, the cost of the D flip-flop is counted as half a package. A brute force conversion to ECL gates was used to generate the circuit of *Figure 3-35b;* cost went up to about three packages. When the wired-OR connection *(Figure 3-35c)* was utilized, the package count dropped back to 2 1/2, and a level of gate delay was eliminated. Sometimes, wiring constraints may limit the usefulness of the wired-OR connection; check wiring rules given in Chapter 5.



a. Original TTL Function, About 2-1/2 Packages



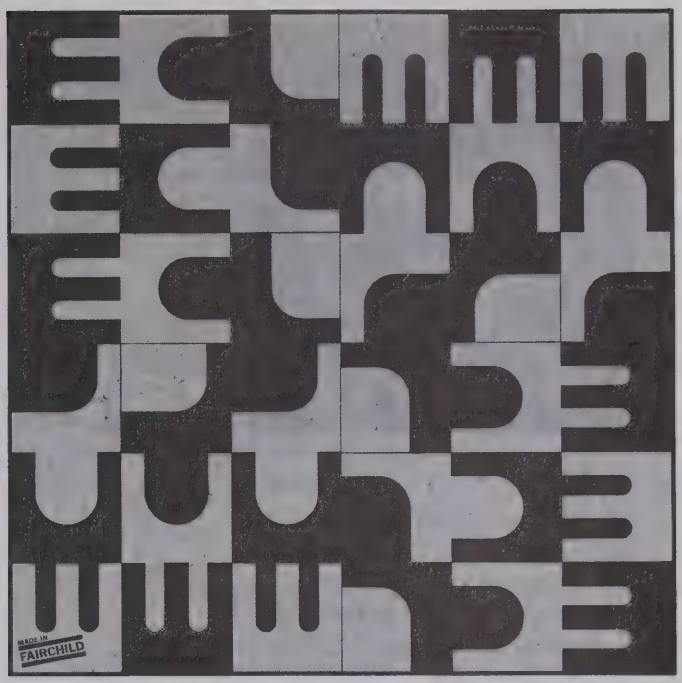
b. Brute Force Conversion to ECL, About 3 Packages



c. Conversion to ECL using Wired-OR, About 2-1/2 Packages

Fig. 3-35. Examples of Conversion of TTL to ECL

THE ECL HANDBOOK SECTION SELECTOR



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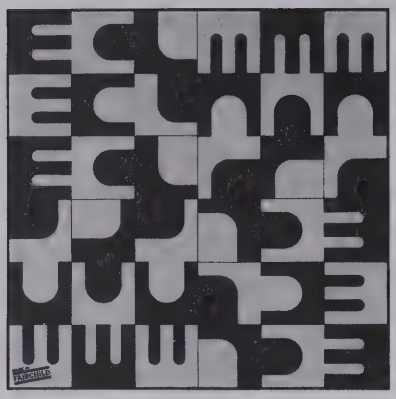
F10K Voltage Compensated ECL Series 7

F95K Fully Compensated ECL Series 8



CHAPTER 4

- Simplifying Assumptions
- Characteristic Impedance
- Propagation Velocity
- Termination and Reflection
- Source Impedance, Multiple Reflections
- Lattice Diagram
- Shorted Line
- Series Termination
- Extra Delay with Termination Capacitance
- Distributed Loading Effects on Line Characteristics
- Mismatched Lines
- Rise Time Versus Line Delay
- Ringing

TRANSMISSION LINE CONCEPTS

INTRODUCTION

The interactions between wiring and circuitry in high speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuits, normalized pulse amplitudes are used in sample waveforms and calculations.

SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors has a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows.

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad (4\text{-}1)$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in henries, C_0 in farads.

PROPAGATION VELOCITY

Propagation velocity v and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, all having the same unit of length.

$$v = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad (4\text{-}2)$$

Equations 4-1 and *4-2* provide a convenient means of determining the L_0 and C_0 of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_0 and C_0, combine *Equations 4-1* and *4-2*.

$$L_0 = \delta Z_0 \qquad (4\text{-}3)$$

$$C_0 = \frac{\delta}{Z_0} \qquad (4\text{-}4)$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1–3]

TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in *Figure 4-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave

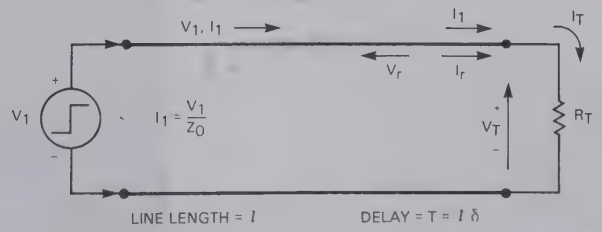


Fig. 4-1. Assigned Polarities and Directions for Determining Reflections

is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated, by V_r and I_r in *Figure 4-1,* starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \qquad (4\text{-}5)$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true.

$$V_1 + V_r = V_T$$

thus $$I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \qquad (4\text{-}6)$$

also $$I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_0}\right)$$

$$V_r = V_1\left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1 \qquad (4\text{-}7)$$

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between –1 and +1 respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 4-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r$$

then $$V_T = V_1(1 + \rho_L) \qquad (4\text{-}8)$$

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 4-8* gives

$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \qquad (4\text{-}9)$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

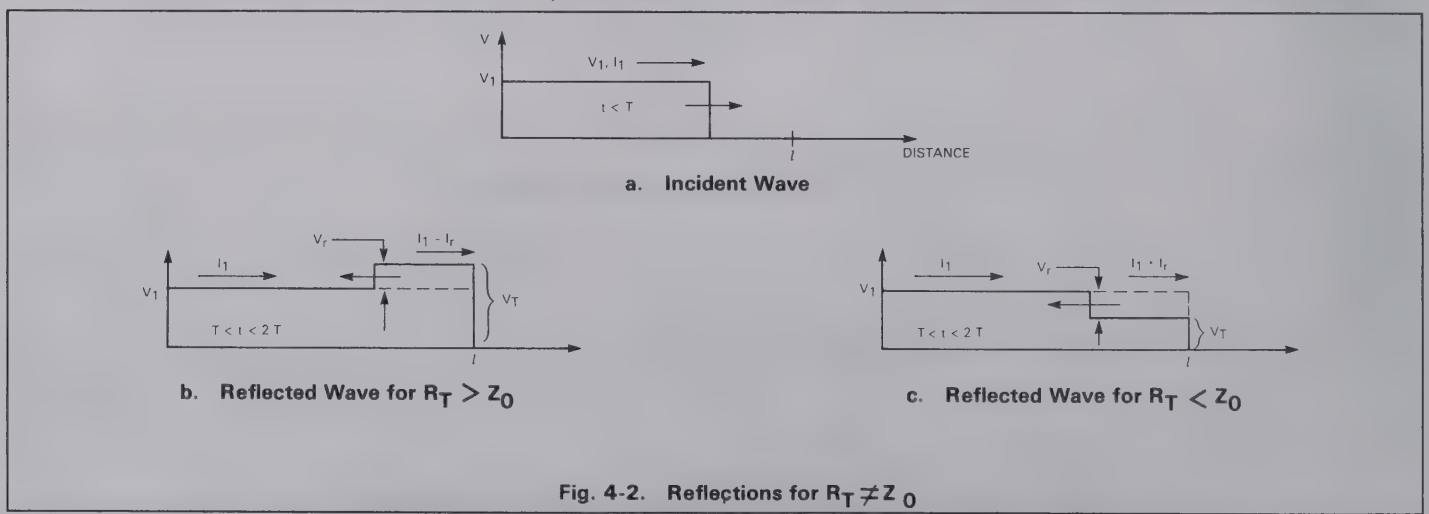
The arrow indicating the direction of V_r in *Figure 4-1,* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 4-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_1 is larger than the final quiescent current, dictated by V_1 and R_T. Hence I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, *i.e.,* R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 4-2* for both cases of mismatch between R_T and Z_0.

The incident wave is shown in *Figure 4-2a,* before it has reached the end of the line. In *Figure 4-2b,* a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 4-2c,* the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.

SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the



a. Incident Wave

b. Reflected Wave for $R_T > Z_0$

c. Reflected Wave for $R_T < Z_0$

Fig. 4-2. Reflections for $R_T \neq Z_0$

response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \qquad (4\text{-}10)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \qquad (4\text{-}11)$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 4-3.* The source is a step function of 1 V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75 V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 4-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 4-3)* to 13 Ω increases ρ_S to –0.75, and the effects are illustrated in *Figure 4-4.* The initial value of V_T is 1.8 V with a reflection of 0.9 V from the open end. When this reflection reaches the source, a reflection of 0.9 x –0.75 V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9 x –0.75 V starts back toward the source. This negative increment is again multiplied by –0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

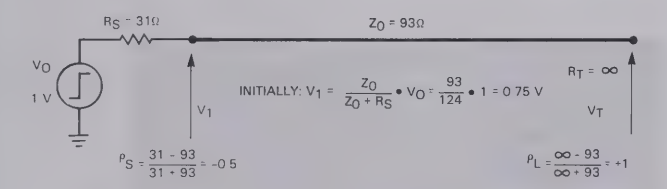
$$V_T - V_T' = (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho_L^2 \rho_S^2$$
$$= (1 + \rho_L) V_1 (1 - \rho_L^2 \rho_S^2) \qquad (4\text{-}12)$$

The factor $(1 - \rho_L^2 \rho_S^2)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating line conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 4-3* is shown in *Figure 4-5.*

The vertical lines symbolize the discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T.



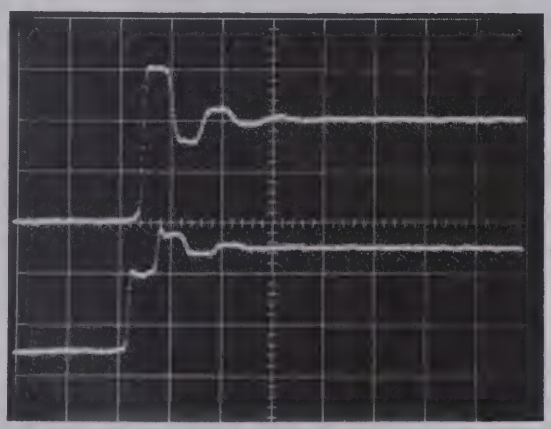


Fig. 4-3. Multiple Reflections Due to Mismatch at Load and Source

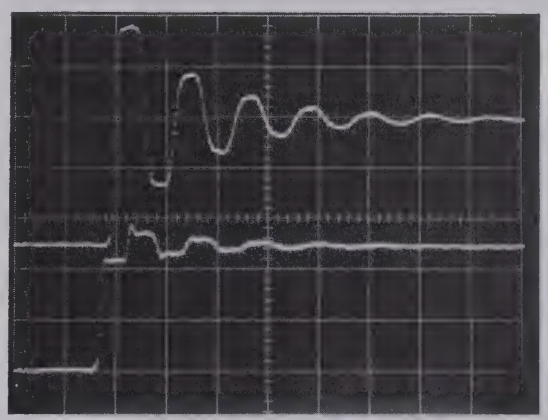


Fig. 4-4. Extended Ringing when R_S of Figure 4-3 is Reduced to 13Ω

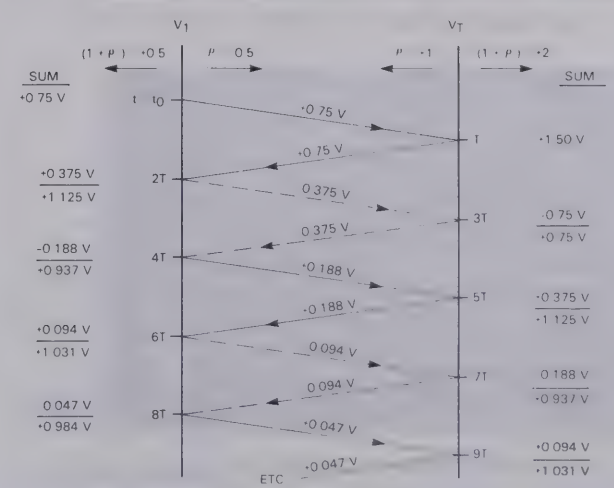


Fig. 4-5. Lattice Diagram for the Circuit of Figure 4-3

The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and $(1+\rho)$ at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1 V, as they must with a 1 V source driving an open-ended line.

SHORTED LINE

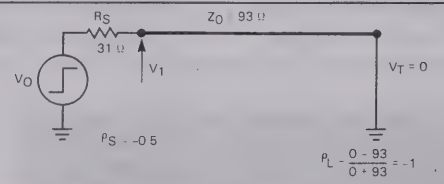
The open-ended line in *Figure 4-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of –1 and successive reflections must cause the line conditions to approach the steady state condition of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 4-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 4-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75 V, which is inverted at the shorted end and returned toward the source as –0.75 V. Arriving back at the source end of the line, this voltage is multiplied by $(1+\rho_S)$, causing a –0.37 V net change in V_1. Concurrently, a reflected voltage of +0.37 V (–0.75 V times ρ_S of –0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

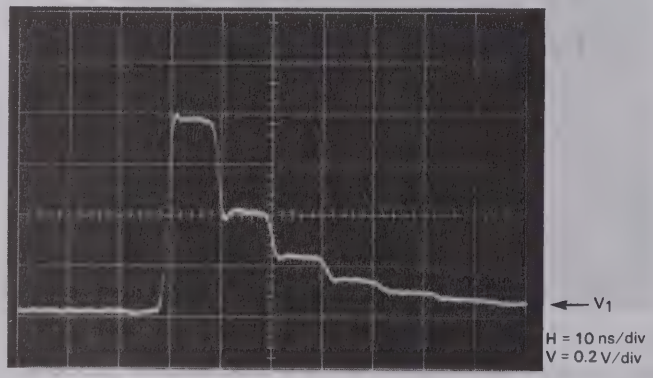
When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 4-6c*. The amplitude decreases by 50% with each successive occurrence as it also did in *Figure 4-6b*.

SERIES TERMINATION

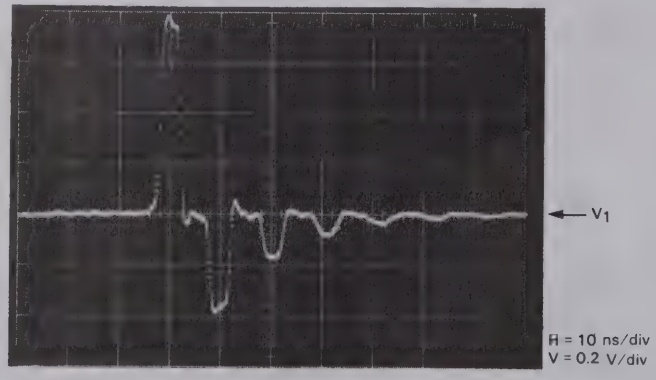
Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 4-7* shows a 93 Ω line driven from a 1 V generator through a source impedance of 93 Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude



a. Reflection Coefficients for Shorted Line

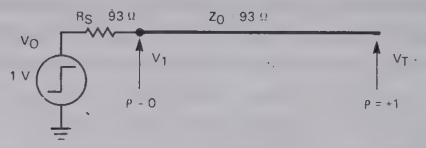


b. Input Pulse Duration ≫ Line Delay



c. Input Pulse Duration < Line Delay

Fig. 4-6. Reflections of Long and Short Pulses on a Shorted Line



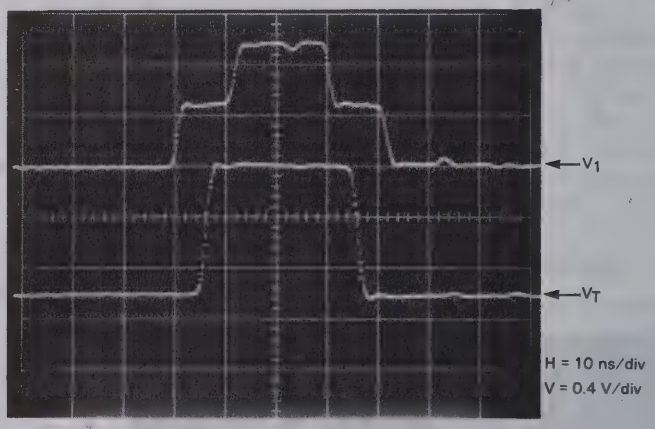


Fig. 4-7. Series Terminated Line and Waveforms

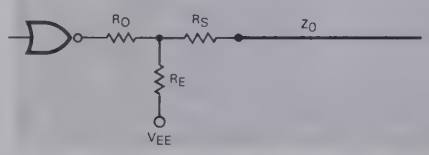


Fig. 4-8. ECL Element Driving a Series Terminated Line

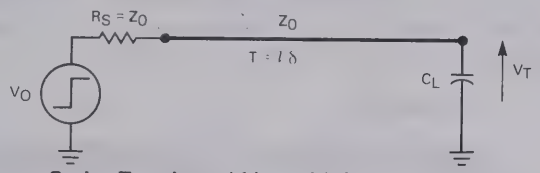
$(1 + \rho_L = 2)$. The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull down resistor to V_{EE}, as indicated in *Figure 4-8*. The resistor R_O shown in *Figure 4-8* symbolizes the output resistance of the ECL gate. The relationships between R_O, R_S, R_E and Z_O are discussed in Chapter 5.

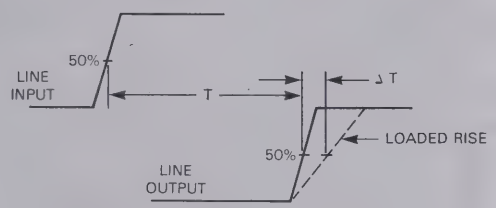
EXTRA DELAY WITH TERMINATION CAPACITANCE

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 4-9* shows how the output waveform changes with increasing load capacitance. *Figure 4-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.

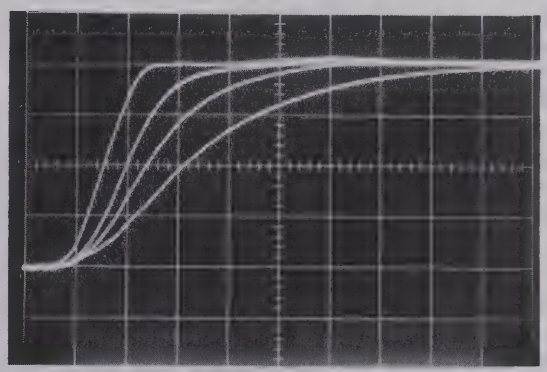
The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 4-10*. One general solution serves both series and parallel termination cases by using an impedance Z' and a time constant τ, defined in *Figure 4-10a* and *4-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At larger ratios of τ /a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 4-11*, based on measured values, shows the increase in delay to the 50% point as a function of the



a. Series Terminated Line with Load Capacitance

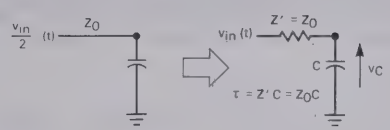


c. Extra Delay ΔT Due to Rise Time Increase

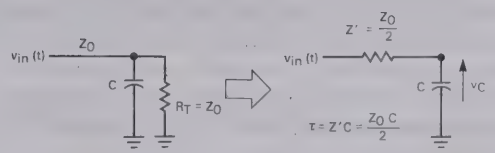


b. Output Rise Time Increase with Increasing Load Capacitance

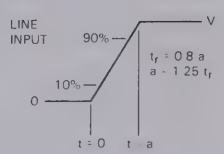
Fig. 4-9. Extra Delay with Termination Capacitance



a. Thevenin Equivalent for Series Terminated Case



b. Thevenin Equivalent for Parallel Terminated Case



$$v_{in}(t) = \frac{V}{a}\ [tu(t) - (t-a)u\ (t-a)]$$

$$u(t) = \begin{matrix} 0 \text{ for } t < o \\ 1 \text{ for } t > o \end{matrix}$$

$$u(t-a) = \begin{matrix} 0 \text{ for } t < a, \\ 1 \text{ for } t > a \end{matrix}$$

$$V_{IN}(S) = \frac{V}{as^2}\ (1 - e^{-as})$$

$$V_C(S) = \frac{V}{a\tau} \cdot \frac{1}{s^2\ (s + 1/\tau)}\ (1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}\ [t - \tau(1 - e^{-t/\tau})]\ u(t) - \frac{V}{a}\ [(t-a) - \tau(1 - e^{-\frac{t-a}{\tau}})]\ u(t-a)$$

c. Equations for Input and Output Voltages

Fig. 4-10. Determining the Effect of End-of-line Capacitance

Z'C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100 Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 4-10a,* Z' is equal to 100 Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is $0.8\,t_r$, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100 Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z' would be 50 Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50 Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.

DISTRIBUTED LOADING EFFECTS ON LINE CHARACTERISTICS

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 4-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 4-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 4-12b,* the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at ≈ −10%) for half its duration. This is about the same reflection that would occur if the 93 Ω line had a middle section with an impedance reduced to 75 Ω.

With a number of capacitors distributed all along the line of *Figure 4-12a,* the combined reflections modify the observed input waveform as shown in the top trace of *Figure 4-12c.* The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T > Z_0$). This analogy is strengthened by observing the effect of reducing R_T from 93 Ω to 75 Ω, which leads to the middle waveform of *Figure 4-12c.* Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 4-12c* the source resistance R_S is reduced from 93 Ω to 75 Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 4-1* to determine the reduced line impedance Z'_0.

$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}}$$

$$Z'_0 = \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \qquad (4\text{-}13)$$

In the example of *Figure 4-12c,* the total load capacitance is 33 pF while the total intrinsic line capacitance C_0 is 60 pF (note that the ratio C_D/C_0 is the same as C_L/lC_0). The calculated value of the reduced impedance is thus.

$$Z'_0 = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\ \Omega \qquad (4\text{-}14)$$

This correlates with the results observed in *Figure 4-12c* when R_T and R_S are reduced to 75 Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 4-2.*

$$\delta' = \sqrt{L_0(C_0 + C_D)} = \sqrt{L_0 C_0}\ \sqrt{1 + \frac{C_D}{C_0}}$$

$$= \delta \sqrt{1 + \frac{C_D}{C_0}} \qquad (4\text{-}15)$$

The line used in the example of *Figure 4-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 4-15.*

$$l\delta' = l\delta\ \sqrt{1.55} = 6\ \sqrt{1.55} = 7.5\ ns \qquad (4\text{-}16)$$

Equation 4-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 4-9.*[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \qquad (4\text{-}17)$$

MISMATCHED LINES

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted pair, line impedance changes run about 5 to 10% and

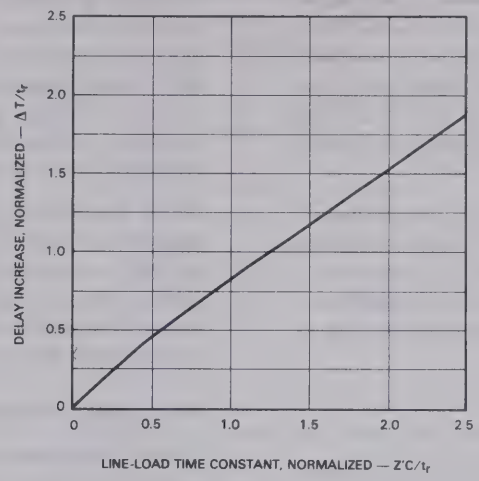
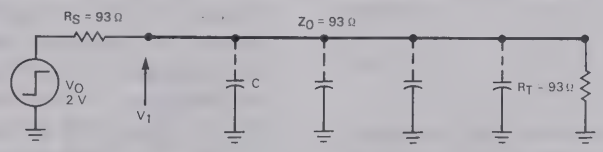
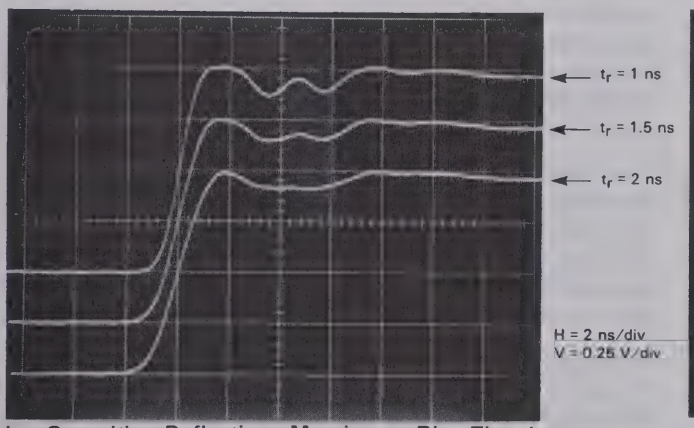


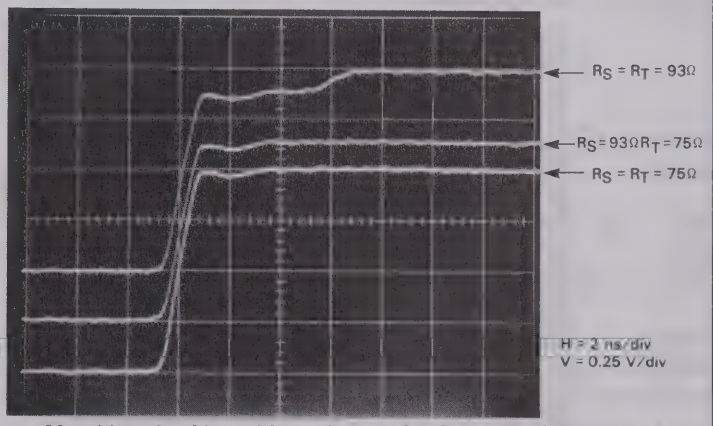
Fig. 4-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to t_r



a. Arrangement for Observing Capacitive Loading Effects

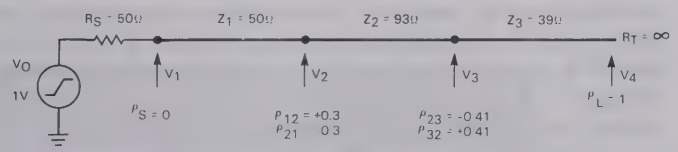


b. Capacitive Reflections Merging as Rise Time Increases



c. Matching the Altered Impedance of a Capacitively Loaded Line

Fig. 4-12. Capacitive Reflections and Effects on Line Characteristics



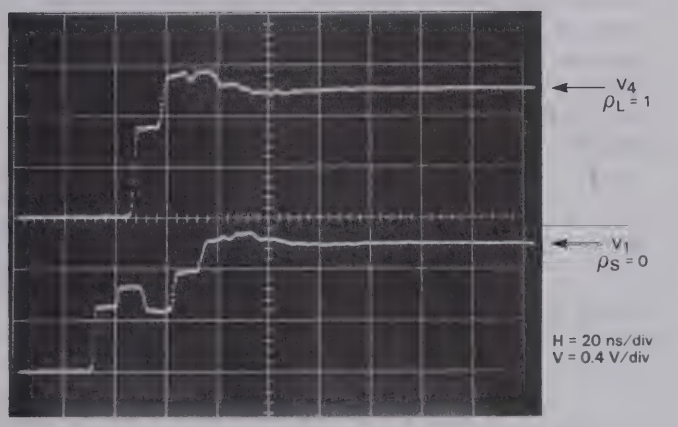


Fig. 4-13. Reflections from Mismatched Lines

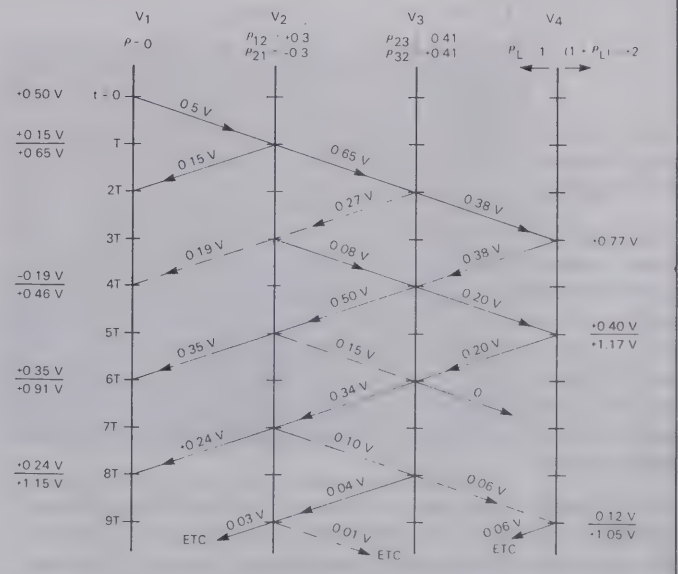


Fig. 4-14. Lattice Diagram for the Circuit of Figure 4-13

reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 4-13* and analyzed in the lattice diagram of *Figure 4-14*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ is determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 4-13,* the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \qquad (4\text{-}18)$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3\ V_1 \qquad (4\text{-}19a)$$

$$V_2 = (1 + \rho_{12})\ V_1 = +1.3\ V_1 \qquad (4\text{-}19b)$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \qquad (4\text{-}20)$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23} V_2 = -0.41\ V_2 = (-0.41)(1.3)\ V_1 = -0.53\ V_1$$

$$V_3 = (1 + \rho_{23})\ V_2 = 0.59\ V_2 = (0.59)(1.3)\ V_1 = 0.77\ V_1 \qquad (4\text{-}21a,b)$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1 + \rho_L)\ V_3 = (1 + \rho_L)(1 + \rho_{23})\ V_2$$

$$= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\ V_1$$

$$= (1 + \rho_L)\ (1 + \rho_{23})\ (1 + \rho_{12})\ \frac{V_O}{2}$$

$$V_4 = (1 + \rho_{23})\ (1 + \rho_{12})\ V_O \qquad (4\text{-}22)$$

Thus, *Equation 4-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 4-13* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time, therefore the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 4-14).*

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 4-15* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 4-15*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.

RISE TIME VERSUS LINE DELAY

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 4-16,* which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 4-16b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1 V. At time T later, V_T rises to 0.5 V. *i.e.,* $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of −0.4 V, *i.e.,* $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1 V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 4-16c,* the input rise time (0 to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 4-16d,* with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 4-16e,* which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 4-16d* can be calculated by starting with the 1 V input ramp.

$$V_1 = \frac{1}{t_r} \cdot t \quad \text{for } 0 \leqslant t \leqslant 4T$$

$$= 1\ V \quad \text{for } t \geqslant 4T \qquad (4\text{-}23)$$

the reflection from the end of the line is

$$V_r = \frac{\rho_L\ (t - 2T)}{t_r} \qquad (4\text{-}24)$$

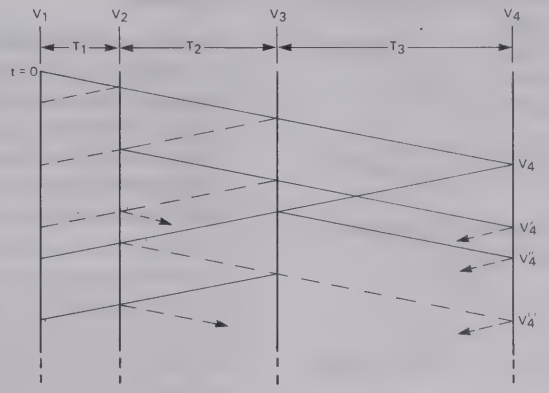
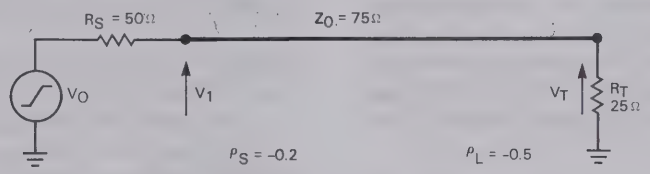
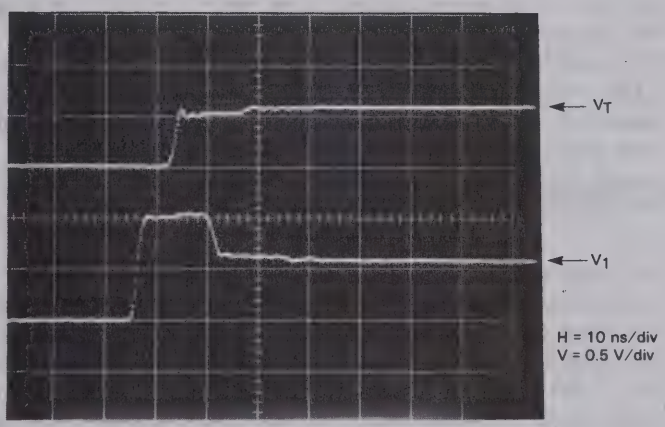


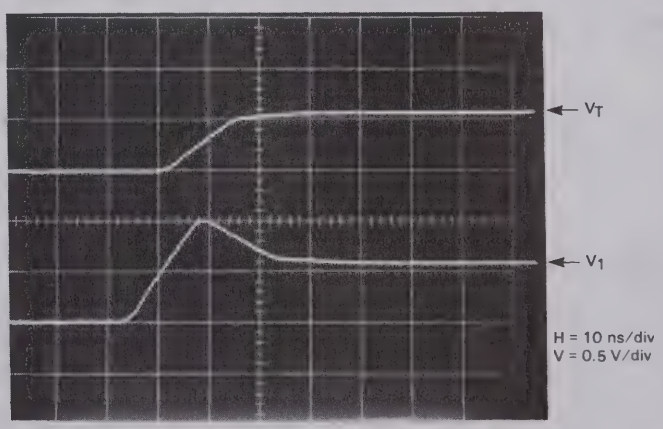
Fig. 4-15. Lattice Diagram for Three Lines with Delay Ratios 1:2:3



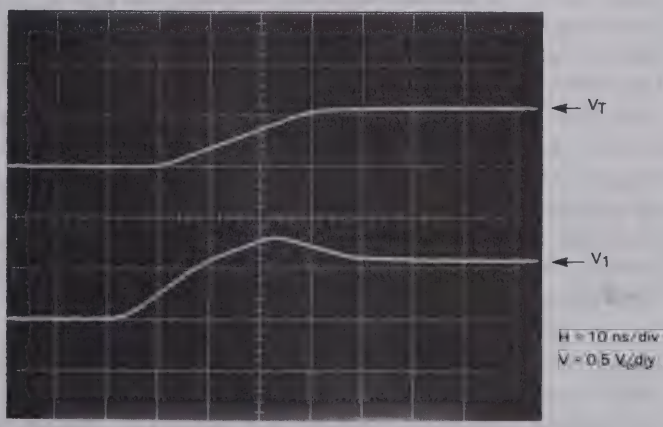
a. Test Arrangement for Rise Time Analysis



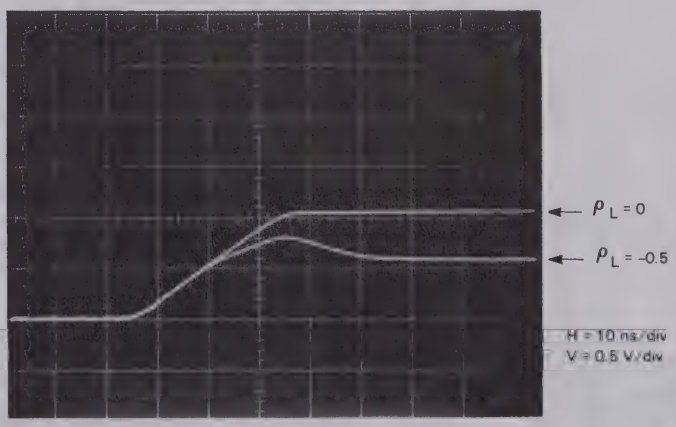
b. Line Voltages for $t_r \ll T$



c. Line Voltages for $t_r = 2T$



d. Line Voltages for $t_r = 4T$



e. Input Voltage With and Without Reflection

Fig. 4-16. Line Voltages for Various Ratios of Rise Time to Line Delay

the portion of the reflection that appears at the input is

$$V_r' = \frac{(1+\rho_S)\,\rho_L\,(t-2T)}{t_r} \qquad (4\text{-}25)$$

the net value of the input voltage is the sum.

$$V_1' = \frac{t}{t_r} + \frac{(1+\rho_S)\,\rho_L\,(t-2T)}{t_r} \qquad (4\text{-}26)$$

The peak value of the input voltage in *Figure 4-16d* is determined by substituting values and letting t equal 4T.

$$V_1' = 1 + \frac{(0.8)\,(-0.5)\,(4T-2T)}{t_r}$$
$$= 1 - 0.4\,(0.5) = 0.8\ V \qquad (4\text{-}27)$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V'_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

$$V'_{1(t)} = V_{1(t)} \qquad for\ 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1+\rho_S)\,\rho_L V_{1(t-2T)} \qquad for\ 2T < t < 4T$$

$$V'_{1(t)} = V_{1(t)} + (1+\rho_S)\,\rho_L V_{1(t-2T)} + (1+\rho_S)\,\rho_S\rho_L{}^2 V_{1(t-4T)} \qquad for\ 4T < t < 6T$$

$$V'_{1(t)} = V_{1(t)} + (1+\rho_S)\,\rho_L V_{1(t-2T)} + (1+\rho_S)\,\rho_S\rho_L{}^2 V_{1(t-4T)} + (1+\rho_S)\,\rho_S{}^2\rho_L{}^3 V_{1(t-6T)} \qquad for\ 6T < t < 8T$$

$$etc. \qquad (4\text{-}28)$$

The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \qquad for\ 0 < t < T$$

$$V_{T(t)} = (1+\rho_L)\,V_{1(t-T)} \qquad for\ T < t < 3T$$

$$V_{T(t)} = (1+\rho_L)\,V_{1(t-T)} + (1+\rho_L)\,\rho_S\rho_L V_{1(t-3T)} \qquad for\ 3T < t < 5T$$

$$V_{T(t)} = (1+\rho_L)\,V_{1(t-T)} + (1+\rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1+\rho_L)\,\rho_S{}^2\rho_L{}^2 V_{1(t-5T)} \qquad for\ 5T < t < 7T$$

$$etc. \qquad (4\text{-}29)$$

RINGING

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 4-17*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is +1 and the source reflection coefficient is assumed to be –0.8, *i.e.*, $R_O = Z_O/9$.

Figure 4-17b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_{O1} rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by –0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to –1.6B at time 2T+A. The negative-going increment also generates a reflection of amplitude –0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T+A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.

In *Figure 4-17c,* the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (*i.e.,* 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 4-17c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 4-17*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increments is zero.

SUMMARY

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept. Mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, *i.e.,* at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

REFERENCES:

1. Metzger, G. and Vabre, J., Transmission Lines with Pulse Excitation, Academic Press, (1969).

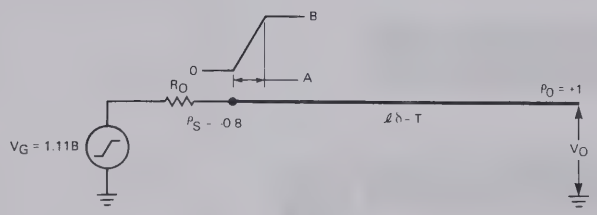
2. Skilling, H., Electric Transmission Lines, McGraw-Hill, (1951).

3. Matick, R., Transmission Lines for Digital and Communication Networks, McGraw-Hill, (1969).

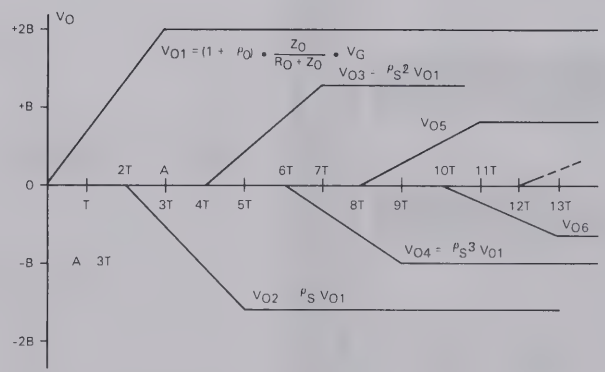
4. Millman, J. and Taub, H., Pulse, Digital and Switching Waveforms, McGraw-Hill, (1965).

5. "Time Domain Reflectometry", Hewlett-Packard Journal, Vol. 15, No. 6, (February 1964).

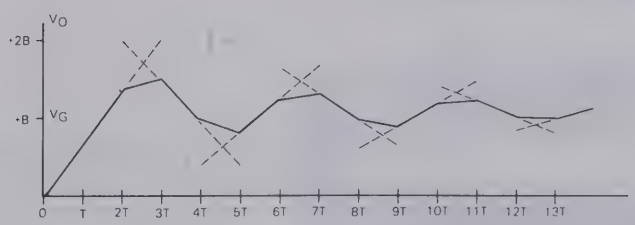
6. Feller, A., Kaupp, H., and Digiacoma, J., "Crosstalk and Reflections in High Speed Digital Systems", Proceedings, Fall Joint Computer Conference, (1965).



a. Ramp Generator Driving Open-ended Line



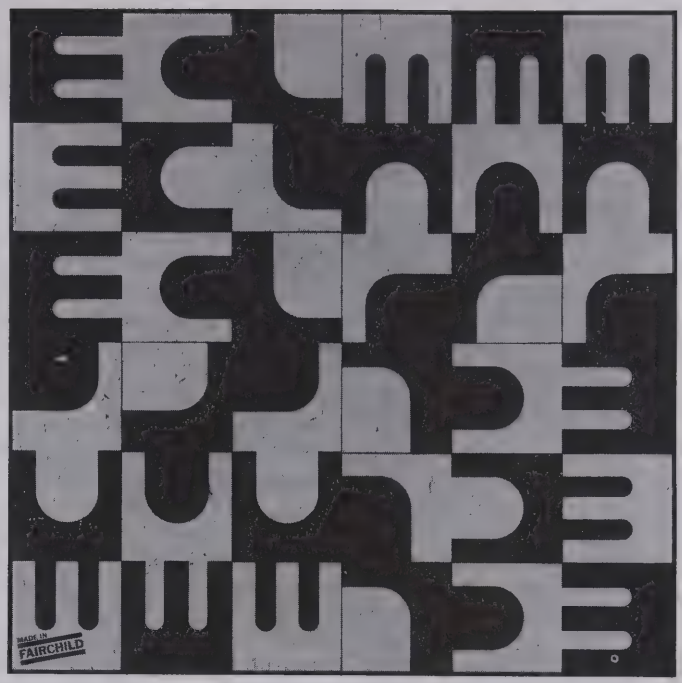
b. Increments of Output Voltage Treated Individually



c. Net Output Signal Determined by Superposition

Fig. 4-17. Basic Relationships Involved in Ringing

THE ECL HANDBOOK SECTION SELECTOR



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CHAPTER 5

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ECL INTERCONNECTIONS

INTRODUCTION

F10K and F95K input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Guidelines and recommendations are intended to help the designer achieve good system performance, consistent with conservative design practice.

PC BOARD TRANSMISSION LINES

Strictly speaking, transmission lines are not required with the relatively slow edge speeds of F10K and F95K ECL, but when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 5-1.* Stripline requires multilayer construction techniques, while microstrip uses ordinary double-clad boards.

Stripline is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 12 layers have been used in ECL systems.

Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 5-1a,* the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 5-1c.*

Microstrip

Equation 5-1 relates microstrip characteristic impedance, dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\ \epsilon_r + 0.67}}\right) \ln \left(\frac{4\,h}{0.67\,(0.8\,w + t)}\right)$$

$$= \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln \left(\frac{5.98\,h}{0.8\,w + t}\right) \qquad (5\text{-}1)$$

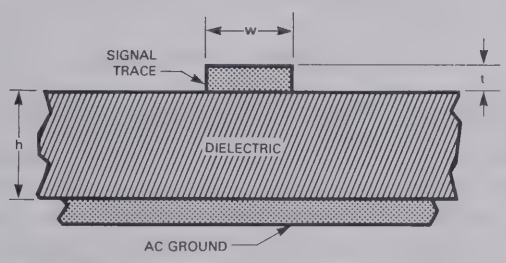
where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air

Equation 5-1 was developed from the impedance formula for a wire over ground plane transmission line, *Equation 5-2.*

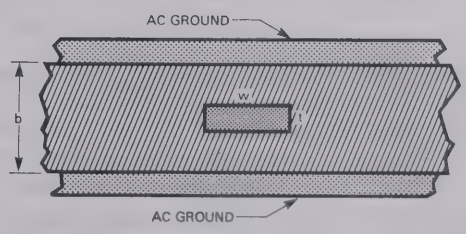
$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln \left(\frac{4\,h}{d}\right) \qquad (5\text{-}2)$$

where d = wire diameter, h = distance from ground to wire center

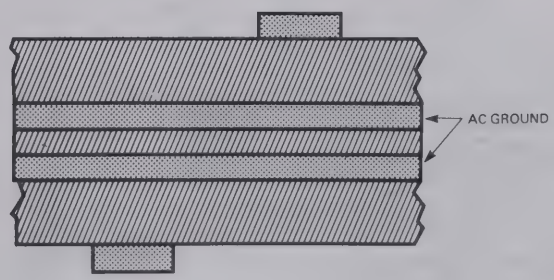
Comparing *Equations 5-1* and *5-2,* the term 0.67 (0.8w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by



a. Microstrip



b. Stripline



c. Composite Microstrip

Fig. 5-1. Transmission Lines on Circuit Boards

measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \bullet \sqrt{\epsilon_r} \quad ns/ft \qquad (5\text{-}3)$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04. Using this value in *Equation 5-1, Figure 5-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 5-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, *(Equation 4-15).*

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

Stripline

Stripline conductors are totally imbedded.. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. *Equation 5-4* is used to calculate stripline impedances.[1-2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln \left(\frac{4b}{0.67\,(0.8\,w + t)}\right) \qquad (5\text{-}4)$$

where b = distance between ground planes, w = trace width, t = trace thickness, $w/(t\text{-}b) < 0.35$ and $t/b < 0.25$

Figure 5-4 shows stripline impedance as a function of trace width, using *Equation 5-4* and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 5-5.*

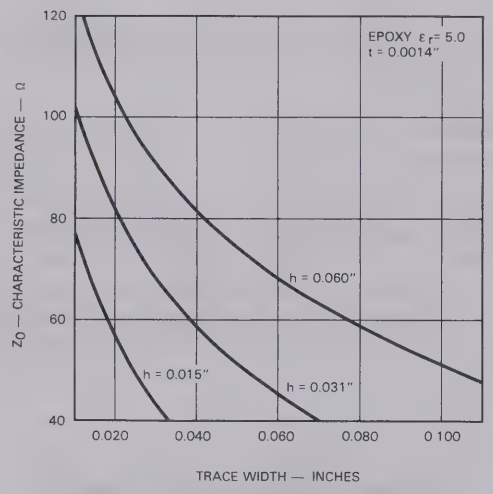


Fig. 5-2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

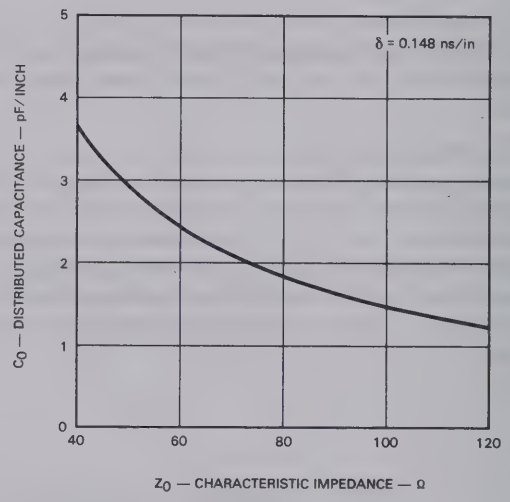


Fig. 5-3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

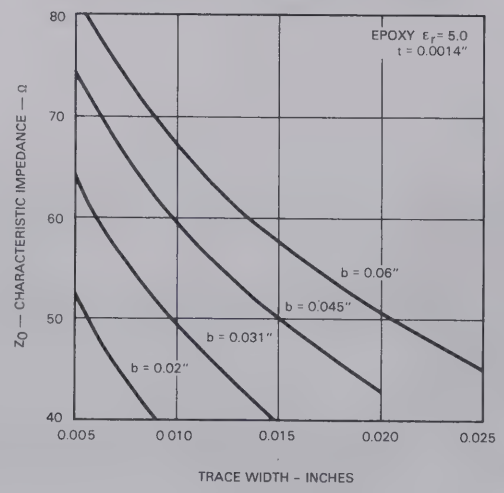


Fig. 5-4. Stripline Impedance Versus Trace Width, G-10 Epoxy

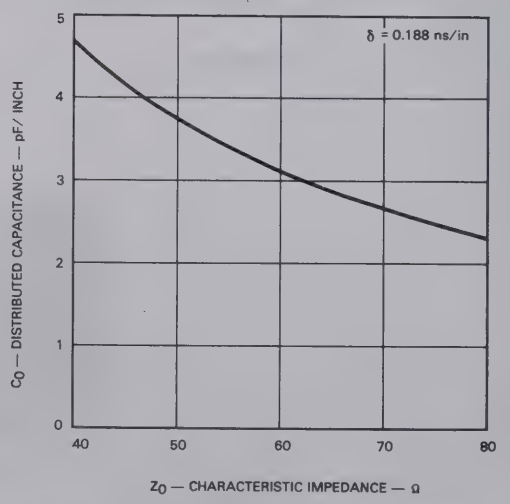


Fig. 5-5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

PARALLEL TERMINATION

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 5-6a.* F10K and F95K circuits do not have internal pull down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A –2 V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can provide the Thevenin equivalent of a single resistor to –2 V if a separate termination supply is not available, *Figure 5-6b.* The average power dissipation in the Thevenin equivalent resistors is about 10 times the dissipation in the single resistor returned to –2 V, as shown in *Figure 6-14.* For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).

F10K output transistors are designed to drive low impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50Ω load returned to –2 V. This gives nominal output levels of –0.9 V at 22 mA and –1.75 V at 5 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50Ω load, the effective source resistance is approximately 6Ω in the HIGH state and 8 Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 5-6c.* The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6 Ω and 8Ω respectively. The values shown for E_{OH} and E_{OL} are determined as follows.

$$E_{OH} = V_{OH} + I_{OH} R_O = -0.90 + (22\ mA)\ (6\ \Omega) = -0.77\ V$$

$$E_{OL} = V_{OL} + I_{OL} R_O = -1.75 + (5\ mA)\ (8\ \Omega) = -1.71\ V$$

using 25°C values of V_{OH} and V_{OL}

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75Ω terminations to –2 V *(Figure 5-6c)* give output levels of approximately –0.94 V and –1.76 V. Noise margins are thus 40 mV less in the HIGH state and 10 mV more in the LOW state, compared to 50 Ω load conditions. Conversely, a single 75Ω load to –2 V causes noise margins 40 mV greater in the HIGH state and 10 mV less in the LOW state, compared to a 50Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad (5\text{-}5)$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2\ R_T}{R_T + Z_0} \qquad (5\text{-}6)$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging *Equation 5-5.*

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad (5\text{-}7)$$

Using 15% reflection limits as examples, the range of R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15}$$

$$1.35 > \frac{R_T}{Z_0} > 0.74 \qquad (5\text{-}8)$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and –19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and –23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the

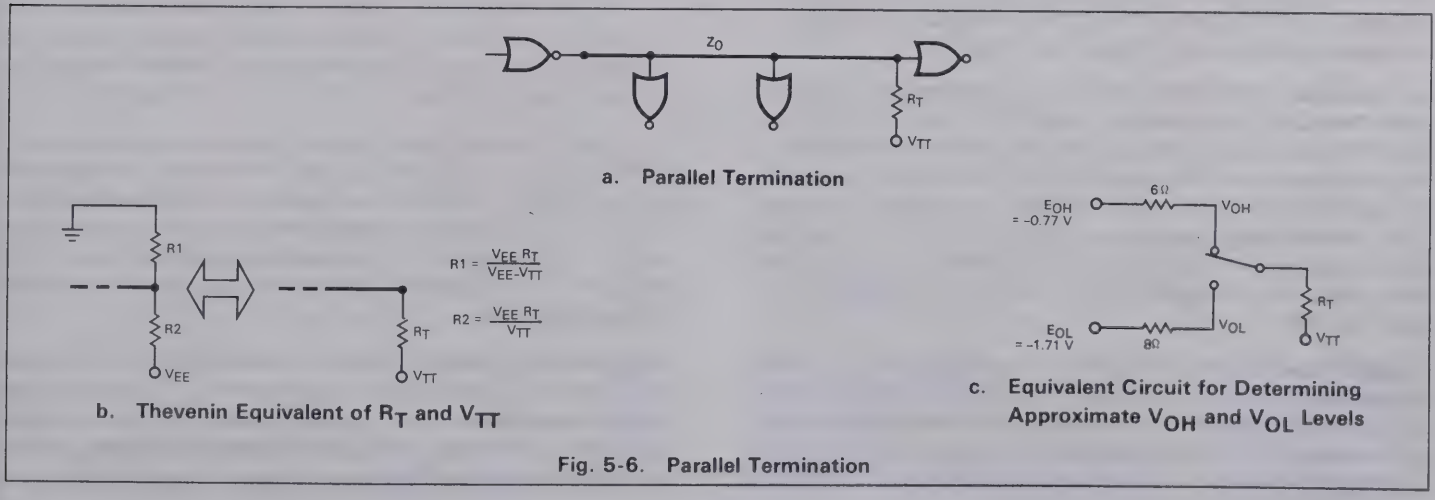


Fig. 5-6. Parallel Termination

emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH} Z_0$.

If the $I_{OH} Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH} Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junction, causing a discontinuous negative-going edge such as the one shown in *Figure 5-17.* In the output LOW state the emitter follower is essentially non-conducting for V_{OL} values more positive than about –1.6 V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 5-6c,* an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH} Z_O > 1.6 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_O + R_T}\right) Z_0 > 1.6 - \left|\frac{V_{TT} R_O + E_{OH} R_T}{R_O + R_T}\right|$$

$$R_T < \frac{(E_{OH} - V_{TT}) Z_0 - (1.6 - |V_{TT}|) R_O}{1.6 - |E_{OH}|} \quad (5\text{-}9)$$

For a V_{TT} of –2 V, R_O of 6 Ω and E_{OH} of –0.77 V, *Equation 5-9* reduces to

$$R_T < 1.48 Z_0 + 2.9\ \Omega$$

For $Z_0 = 50\Omega$, the emitter follower cuts off during a negative-going transition if R_T exceeds 77 Ω. Changing the voltage level criteria to –1.65 V to insure continuous conduction in the emitter follower gives an upper limit of 72 Ω for a 50 Ω line. For a line terminated at the receiving end with a resistance to –2 V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 40%. This insures a satisfactory negative-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

The input impedance of F10K and F95K is predominately capacitive. A single-function input has an effective value of 2.75 pF, as determined by its effect on reflected and transmitted signals on transmission lines. In practical calculations, a value of 3 pF is used. Approximately two-thirds of this capacitance is attributed to the internal circuitry and one-third to the package lead and internal bonding.

An input lead connected to several internal functions exhibits more than 3 pF. For example, the F10101 and F95101 quad OR/NOR gates have a Common Enable input connected internally to four gates. The capacitance for this type of input can be determined by assuming 1 pF for the package lead and 2 pF for each gate input, for a total of 9 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 4. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figures 5-3* and *5-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ *(Equation 5-3)* by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figures 5-10, 5-11, 5-12, 5-13).* The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

SERIES TERMINATION

Series termination requires a resistor between the driver and transmission line, *Figure 5-7.* The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 5-7,* one load is shown connected at point D, away from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated lines *(Figures 5-10, 5-11, 5-12* and *5-13).*

The signal at the end has a slower rise time than the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product of line impedance and load capacitance is discussed in Chapter 4.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 5-7),* which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical

switch which opens to initiate the negative-going swing. At this instant, Z_0 acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.4 V transient into the line, which then doubles at the load end to give 0.8 V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.4}{Z_0} \qquad (5\text{-}10)$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should therefore be ignored when calculating R_E.

Increasing the minimum signal swing into the line 30% to 0.52 V insures sufficient pull down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.52}{Z_0} \qquad (5\text{-}11)$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.82 V. The value of R_S is equal to Z_0 minus R_O (R_O averages 7 Ω). Inserting these values and rearranging *Equation 5-11* gives the following.

$$R_E \leq 6.4\,Z_0 + 7\,\Omega \qquad (5\text{-}12)$$

Power dissipation in R_E is listed in *Figure 6-15,* which shows that dissipation in R_E is greater than in R_T of a parallel termination to –2 V, but less than in the two resistors of the Thevenin equivalent parallel termination.

The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of inputs, with a 265 µA worst-case value for a simple gate input. The voltage drop subtracts from the HIGH state noise margin as outlined in *Figure 5-8a.*

However, there is more HIGH state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50 Ω load to –2 V. This makes V_{OH} more positive; the increase ranges from 60 mV for a 50 Ω line to 100 mV for a 100 Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_O$ (= Z_0) gives the allowed load input current (I_X in *Figure 5-8a*). This works out to 1.2 mA for a 50 Ω line, 1.1 mA for a 75 Ω line, and 1 mA for a 100 Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 2.2 mA, 1.73 mA, and 1.5 mA for 50 Ω, 75 Ω, and 100 Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 5-8b,* if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_O. This voltage drop decreases the HIGH state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application. The appropriate R_E value can be determined using *Equation 5-13.*

$$\frac{1}{R_E} \geq \frac{1}{7.4\,Z_1 - R_{S1}} + \frac{1}{7.4\,Z_2 - R_{S2}} + \frac{1}{7.4\,Z_3 - R_{S3}} \qquad (5\text{-}13)$$

Circuits with multiple outputs (10110, 10111, 95110, 95111) provide an alternate means of driving several lines simultaneously *(Figure 5-8c).* Each output should be treated individually when assigning load distribution, line impedance, and R_E value.

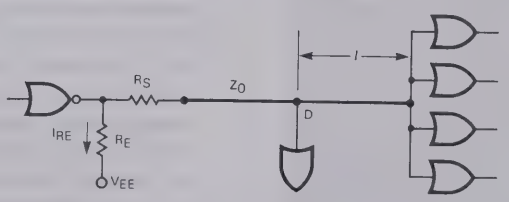
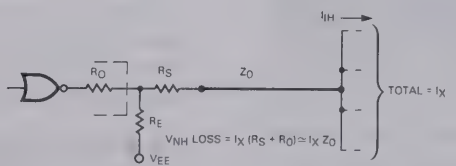
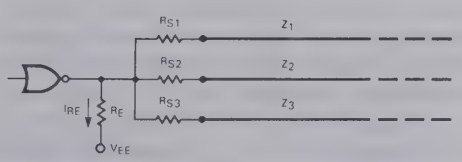


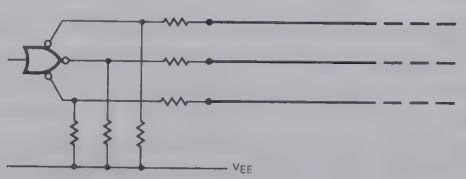
Fig. 5-7. Series Termination



a. Noise Margin Loss Due to Load Input Current



b. Driving Several Lines from One Output



c. Using Multiple Output Element for Load Sharing

Fig. 5-8. Loading Considerations for Series Termination

UNTERMINATED LINES

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately –0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments is the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 4, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 5-9a)* making V_{OH} higher and V_{OL} lower.

For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 4 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2l\delta' = 2l\delta \sqrt{1 + \frac{C_L}{lC_O}}$$

Solving this expression for the line length:

$$l_{max} = \frac{1}{2} \sqrt{\left(\frac{C_L}{C_O}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_O} \qquad (5\text{-}14)$$

The shorter the rise time, the shorter the permissible line length. For F10K and F95K ECL, the minimum rise time from 20% to 80% is specified as 1.5 ns. Using this rise time and 3 pF per fan out load, calculated minimum line lengths for G-10 epoxy microstrip are listed in *Figure 5-10.* Similar line lengths for epoxy stripline are tabulated in *Figure 5-11.* For other combinations of rise time, impedance, fan out or line characteristics (δ and C_O), maximum lengths are calculated using *Equation 5-14.*

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 1.5 ns rise time are listed in *Figure 5-12* for microstrip and in *Figure 5-13* for stripline. For line impedances not listed, linear interpolation can be used to determine appropriate line lengths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/in. is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

Resistor R_E must provide the current for the negative-going signal at the driver output. The relationships are similar to those for series termination. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 5-9b.* The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 5-9c,* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330 Ω. Changing R_E to 510 Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6 V at the driving end of the line. This gives an upper limit on the value of R_E, as follows.

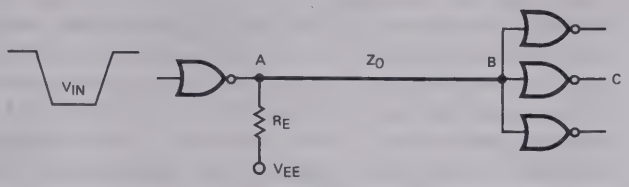
$$\text{initial step} = \Delta I \cdot Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

$$R_E = \leq 6.25\, Z_0 \qquad (5\text{-}15)$$

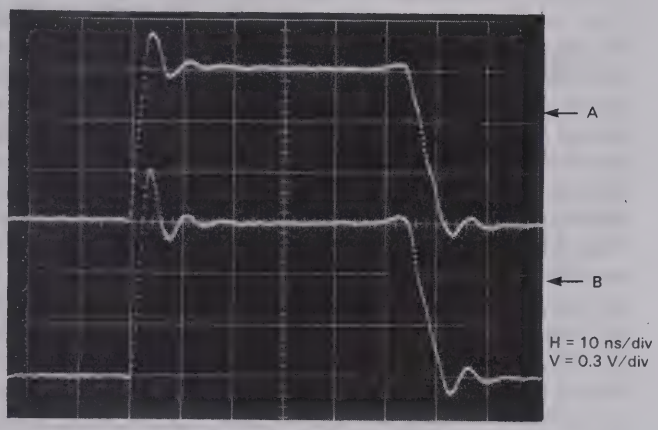
An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from *Equation 5-15,* using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 5-14a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 5-14b.* The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current (through R_T) and the negative-going signal swing was discussed earlier in connection with parallel termination.

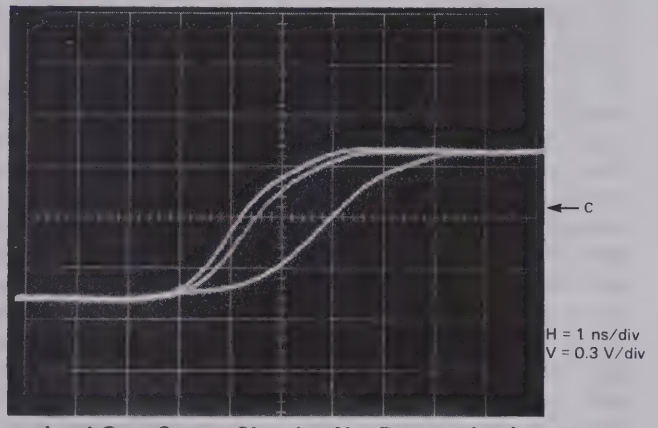
The bottom trace in *Figure 5-14b* shows the effect of connecting two stubs to the driver output. The steps in the trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increases the switching time of the circuit connected to point A. If this extra delay can not be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 5-14a.* The initial negative-going step at point A should be about 0.7 V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7 V. If the driver output is treated as a switch that opens to initiate the negative-going



a. Unterminated Line



b. Line Voltages Showing Stair-Step Trailing Edges



c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330Ω, 510Ω, 1 kΩ

Fig. 5-9. Effect of R_E Value on Trailing Edge Propagation

Z_0	Number of Fan Out Loads				
	2	3	4	6	8
50	4.15*	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in., distributed loading.

Fig. 5-10. Maximum Worst-case Line Lengths for Unterminated Microstrip.

Z_0	Number of Fan Out Loads				
	2	3	4	6	8
50	3.30*	3.00	2.70	2.25	1.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

*length in inches.
Unit load = 3 pF; δ = 0.188 ns/in., distributed loading.

Fig. 5-11. Maximum Worst-case Line Lengths for Unterminated Stripline.

Z_0	Number of Fan Out Loads				
	1	2	4	6	8
50	4.40*	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

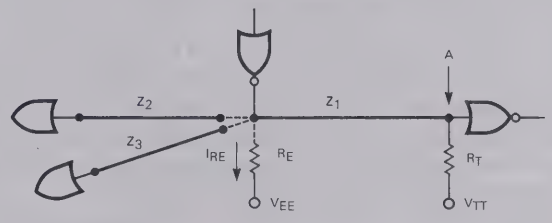
*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in., concentrated loading.

Fig. 5-12. Maximum Worst-case Line Lengths for Unterminated Microstrip.

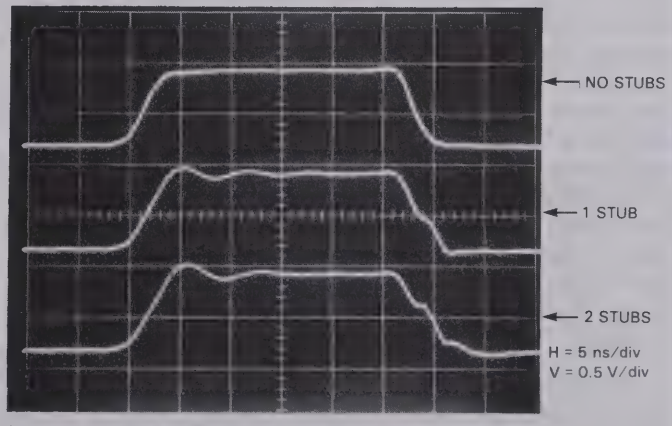
Z_0	Number of Fan Out Loads				
	1	2	4	6	8
50	3.45*	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

*length in inches.
Unit load = 3 pF; δ = 0.188 ns/in., concentrated loading.

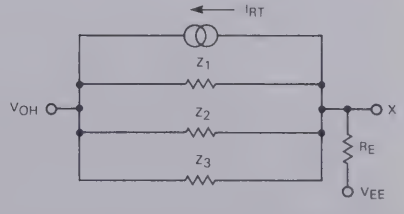
Fig. 5-13. Maximum Worst-case Line Lengths for Unterminated Stripline.



a. Multiple Lines



b. Waveforms at Termination Point A



c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output

Fig. 5-14. Driving Terminated and Unterminated Lines in Parallel

signal, the equivalent circuit of *Figure 5-14c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z' to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = (|V_{EE}| - |V_{OH}| - |\Delta V|) \cdot \left(\frac{Z'}{|\Delta V| - |I_{RT}|\ Z'}\right) \quad (5\text{-}16)$$

For a sample calculation, assume that R_T and the line impedances are each 100 Ω, V_{OH} is -0.9 V, ΔV is 0.7 and V_{TT} is -2 V. I_{RT} is thus 11 mA and the calculated value of R_E is 366 Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just what stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figures 5-10, 5-11, 5-12 and 5-13.*

DATA BUSSING

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 5-15).* Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. For calculating the modified delay of the line (Chapter 4) the capacitance of a LOW (unselected) driver output should be taken as 2 pF.

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedances less than 100 Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH state noise margin. This loss can be eliminated if necessary by using multiple output gates (10110, 10111, 95110, 95111) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100 Ω line terminated at both ends represents a net 50 Ω dc load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be -1.65 V. If another output with identical dc characteristics shares the load current equally the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW state noise margin is specified greater than the HIGH state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, *i.e.,* the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

WIRED-OR

In general purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which

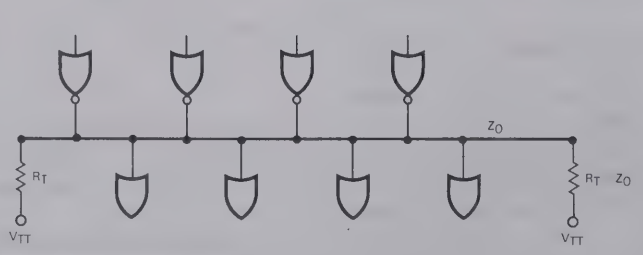


Fig. 5-15. Data Bus or Party Line

in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net result is a "V" shaped negative glitch whose amplitude and duration depend on three factors; current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra waiting time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 16*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.

BACKPLANE INTERCONNECTIONS

Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 6) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150 Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 5-17* illustrates the effects of impedance variations with a 15-inch wire parallel terminated with 150 Ω to –2 V. *Figure 5-17b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane. The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90 Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

Figure 5-17c shows waveforms for a similar arrangement, but with the wire about 1/8 inch from a ground screen. The impedance of the wire is greater than the 150 Ω termination,

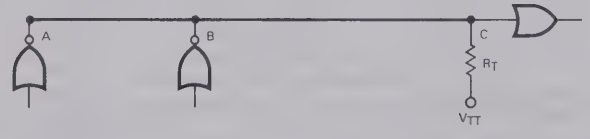
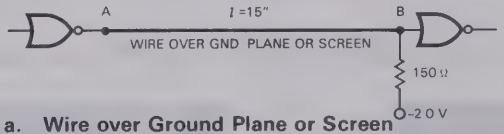
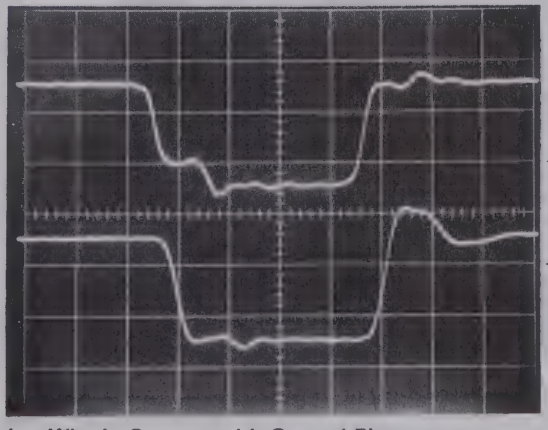


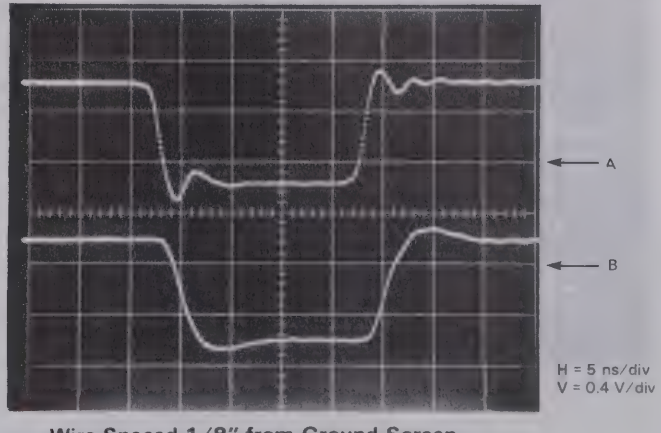
Fig. 5-16. Relative to Wired-OR Propagation



a. Wire over Ground Plane or Screen



b. Wire in Contact with Ground Plane



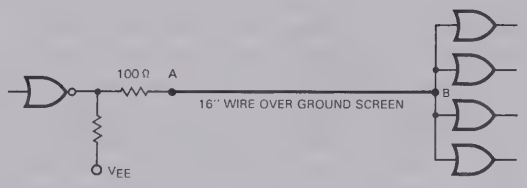
c. Wire Spaced 1/8" from Ground Screen

Fig. 5-17. Parallel Terminated Backplane Wire

but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200 Ω constant impedance line were terminated with 150 Ω.

Series source resistance can also be used with single wire interconnections to absorb reflections. *Figure 5-18* shows a 16-inch wire with a ground screen driven through a source resistance of 100 Ω. The waveforms show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight slope changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from a PC board transmission line. *Figure 5-19a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 5-19b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 5-19c* shows the signals at the input to the driving gate and at the output of a load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 5-19a* is a case of mismatched transmission lines, discussed in Chapter 4.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in



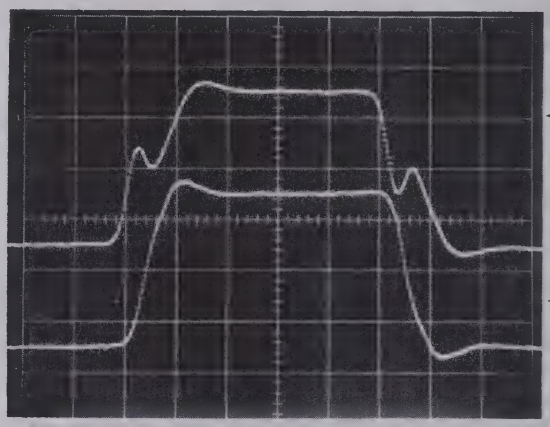
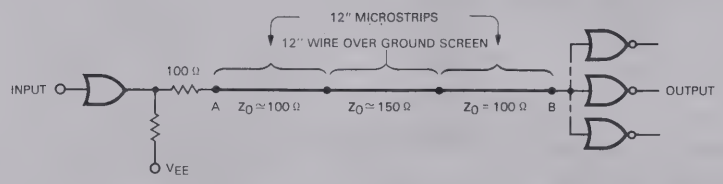
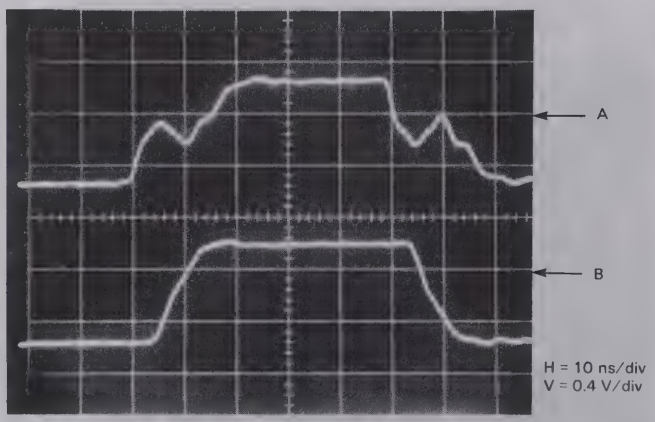


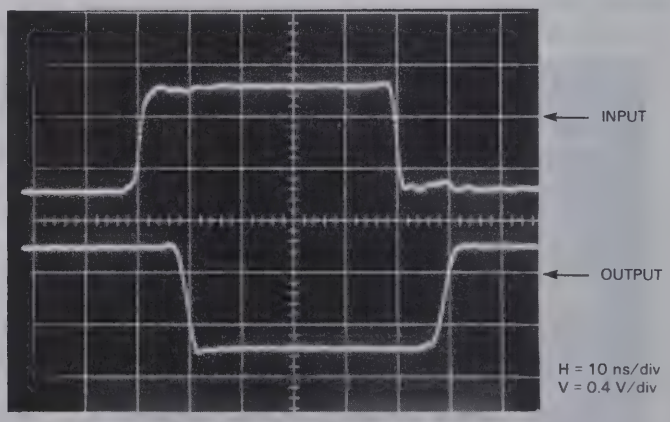
Fig. 5-18. Series Terminated Backplane Wire



a. Backplane Wire Interconnecting PC Board Lines



b. Signals into the First Microstrip and at the Loads



c. Input to Driving Gate and Output of Load Gate

Fig. 5-19. Signal Path with Sequence of Microstrip, Wire, Microstrip

the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall times (Chapter 4) further increasing the effective propagation delay.

Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115 Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 5-20a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

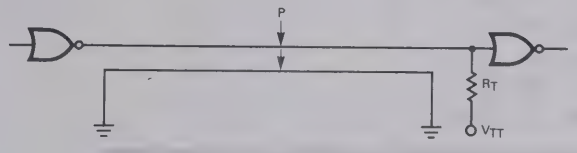
Differential line driving and receiving with a complementary gate as the driver and an F95116 or F10116 line receiver is illustrated in *Figure 20b*. Differential operation provides high noise immunity, since common mode input voltages between -0.55 V and -3.0 V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near higher power transients, shielded twisted pair is recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 20c*.

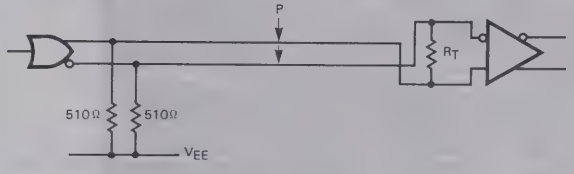
Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on lead 9 or lead 11 of the quad and triple line receivers, respectively.

In the differential mode, a twisted pair can send high frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise time effects on time jitter.[3]

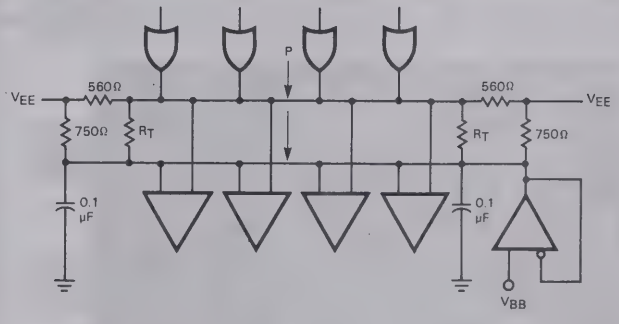
Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 5-21a*, 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 5-21b,c*, the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 5-21c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



a. Single-Ended Twisted Pair

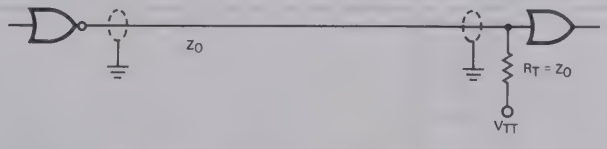


b. Differential Transmission and Reception

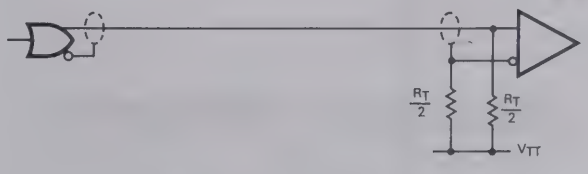


c. Backplane Data Bus

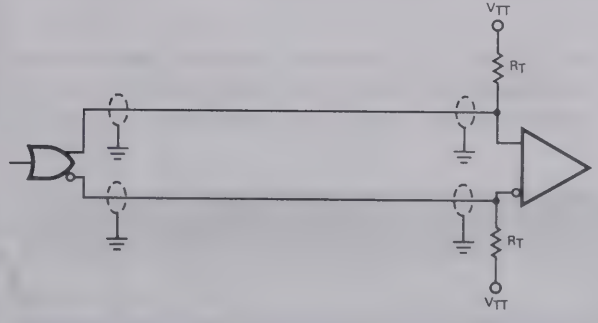
Fig. 5-20. Twisted Pair Connections



a. Single-Ended Coaxial Transmission



b. Differential Coaxial Transmission



c. Differential Transmission with Grounded Shields

Fig. 5-21. Coaxial Cable Connections

*Teflon is a registered trademark of E. I. du Pont de Nemours Company

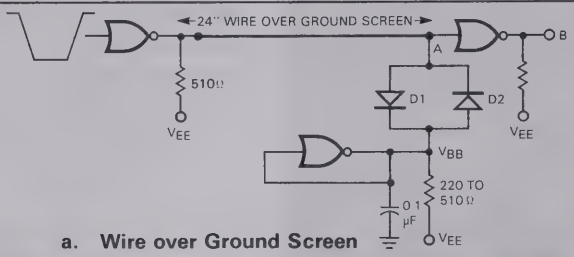
SCHOTTKY DIODE CLAMPING

One method of minimizing ringing at the end of a line involves the use of clamping diodes to limit overshoot, *(Figure 5-22)*. Two diodes are required to limit overshoot on both the positive-going and negative-going edges of the signal. In theory, any type of high speed switching diode could be used, provided each diode is returned to an appropriate reference voltage. Schottky diode forward characteristics *(Figure 5-23)* allow both diodes of a clamping pair to return to the same reference voltage. The required reference voltage is the average of V_{OH} and V_{OL}, which is V_{BB}. This voltage is readily obtained from any ECL gate by connecting its input and output together, since the only voltage which will satisfy both the input and output is the internal reference voltage V_{BB}. In this input-to-output connection, good RF wiring practice and a bypass capacitor are required to prevent oscillation. A pull-down resistor is also required to establish current flow in the output transistor and to sink the steady state current (approximately 1 mA) from D1 when the signal is at the V_{OH} level. A resistor value in the range of 220 to 510 Ω is normally required. If the V_{BB} source is at a distance from the diodes, a bypass capacitor is required at the reference end of the diodes to absorb the transient currents.

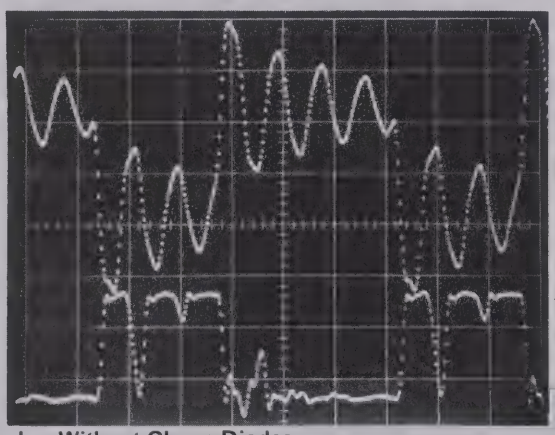
The effectiveness of clamping diode termination can be judged by the waveforms in *Figure 5-22*. Without the diodes, ringing at the input and the effect on the output of the load gate are severe, *(Figure 5-22b)*. With the diodes connected, changes in line current are absorbed by the diodes and ringing is controlled.

REFERENCES

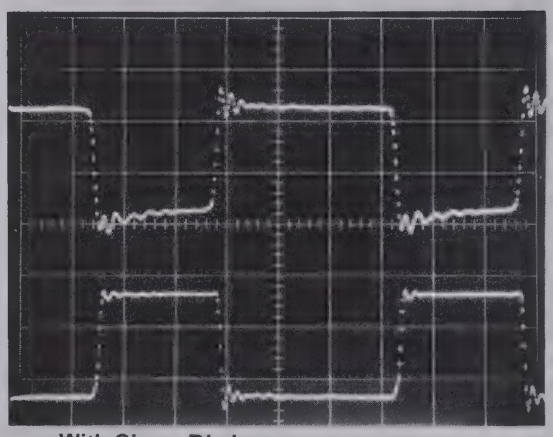
1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," IEEE Transactions on Electronic Computers, Vol. EC-16 (April, 1967).
2. Harper, C. A., Handbook of Wiring, Cabling, and Interconnections for Electronics. New York: McGraw-Hill, 1972.
3. True, K. M., 'Transmission Line Interface Elements," The TTL Applications Handbook, Chapter 14 (August, 1973), pp. 14-1 – 14-14.



a. Wire over Ground Screen



b. Without Clamp Diodes



c. With Clamp Diodes

Fig. 5-22. Limiting Ringing by Clamp Diode Termination

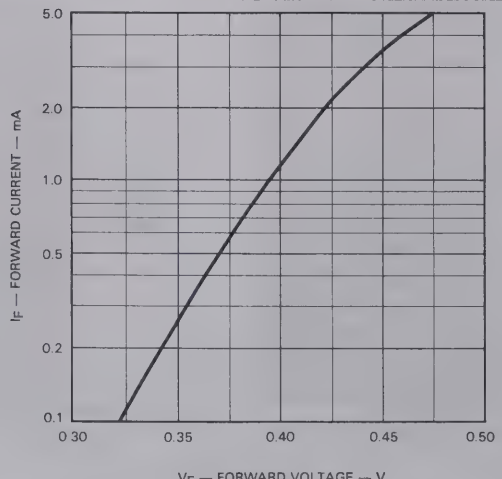
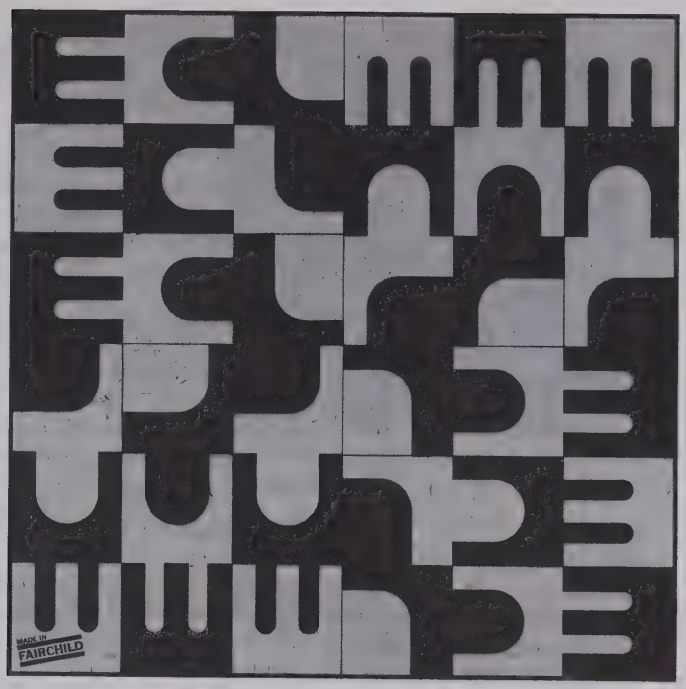


Fig. 5-23. Typical Schottky Diode Forward Characteristics

THE ECL HANDBOOK SECTION SELECTOR



Introduction

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ECL Logic Design 3

Transmission Line Concepts 4

ECL Interconnections 5

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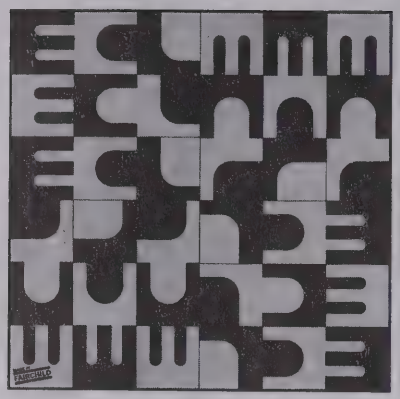
ECL PRODUCT INFORMATION

F10K Voltage Compensated ECL Series 7

F95K Fully Compensated ECL Series 8



CHAPTER 6

- Logic Circuit Ground, V_{CC}
- Conductor Resistances
- Temperature Coefficient
- Distribution Impedance
- Ground on PC Boards
- Backplane Signal Ground
- Termination Supply, V_{TT}
- V_{EE} Supply
- Thermal Considerations

POWER DISTRIBUTION AND THERMAL CONSIDERATIONS

INTRODUCTION

High speed circuits generally consume more power than similar low speed counterparts. At the system level, this means that the supply distribution system must handle a greater magnitude of current flow, while the larger heat load places greater demands on the cooling system. Direct current voltage drops along ground busses affect noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F10K and F95K circuits, but they require careful consideration with conventional 10,000 series ECL. Similarly, temperature gradients are not of concern with F95K circuits, but with F10K or conventional 10,000 circuits, they degrade noise margins for single-ended interconnections.

LOGIC CIRCUIT GROUND, V_{CC}

The positive potential V_{CC} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in Chapter 2. This effect for TTL/DTL circuits as well as for ECL circuits is illustrated in *Figure 6-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW state noise margin of the TTL/DTL circuits and the HIGH state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. Tabulations of ground currents in ECL designs must include termination currents as well as operating currents I_{EE}. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 6-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current i per card, and an incremental bus resistance r between card positions, the bus voltage drops between the various positions can be determined by proceeding as follows.

between positions 1 and 2:

$$v_{1\text{-}2} = (n-1)\,ir$$

between positions 1 and 3:

$$v_{1\text{-}3} = (n-1)\,ir + (n-2)\,ir$$

between positions 1 and 4:

$$v_{1\text{-}4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$$

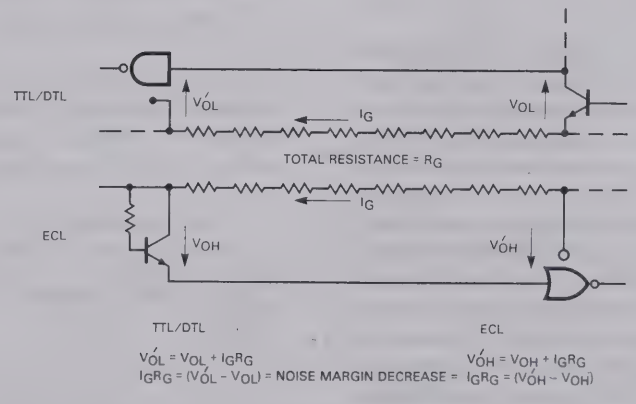


Fig. 6-1. Effect of Ground Resistance on Noise Margins

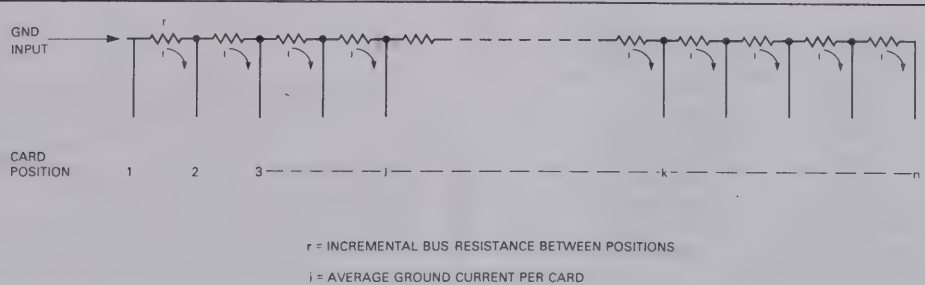


Fig. 6-2. Ground Shift Along a Row of PC Cards

between 1 and n: $v_{1\text{-}n} = ir\ \{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$

$$= ir\ [1 + 2 + 3 + \ldots + (n-1)]$$

$$v_{1\text{-}n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in *Equation 6-1.*

(6-1)

$$v_{1\text{-}15} = ir \sum_{1}^{14} n = ir\ (1 + 2 + 3 + \ldots + 13 + 14) = 105\,ir$$

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j\text{-}k} = (n-j)ir + [n-(j+1)]ir + [n-(j+2)]ir + \ldots + \{n-[j+(k\text{-}j\text{-}1)]\}\ ir$$

$$= (k-j)nir - ir\ \{j + (j+1) + (j+2) + \ldots + [j+(k\text{-}j\text{-}1)]\}$$

$$v_{j\text{-}k} = (k-j)nir - ir \sum_{j}^{k-1} n = ir\,[(k-j)n - \sum_{j}^{k-1} n] \quad (6\text{-}2)$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j\text{-}k} = ir\,[(9-4)15 - (4+5+6+7+8)]$$

$$= ir\,(75-30) = 45\,ir \quad (6\text{-}3)$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10\text{-}15} = ir\,[(15-10)15 - (10+11+12+13+14)]$$

$$= ir\,(75-60) = 15ir \quad (6\text{-}4)$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross sectional area as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential, *i.e.,* twisted pair, transmission and reception method should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

CONDUCTOR RESISTANCES

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 6-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and hence areas is; as gauge numbers increase, resistance doubles with every third gauge number; *e.g.,* the resistance per foot of #10 wire is 1 mΩ; for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships appear as follows.

$$\text{Copper resistivity} = \rho = 1.724 \times 10^{-6}\ \Omega - cm\ @\ 20^{\circ}C$$

$$\text{Resistance of a conductor} = \rho\frac{l}{A} = \rho\frac{l}{tw}$$

where: l = length t = thickness w = width

$$\text{Sheet resistance} = \rho_S = \frac{\rho}{t}\ \Omega\ per\ \frac{l}{w}$$

The length/width ratio l/w is dimensionless; therefore the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares", then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$$\rho(\Omega\text{-}in.) = \rho(\Omega\text{-}cm) \div 2.54 = 6.788 \times 10^{-7}\ \Omega\text{-}in.$$

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 6-4.* Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

$$\text{Sheet resistance } \rho_S = \frac{\rho}{t} = 5.657 \times 10^{-4}\ \Omega\ per\ square$$

The number of squares S for the rectangular sections are as follows.

$$S_1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

AWG B&S Gauge	Resistance mΩ per foot	Cross-sectional Area square inches
#2	0.156	5.213×10^{2}
#6	0.395	2.062×10^{2}
#10	0.999	8.155×10^{3}
#12	1.588	5.129×10^{3}
#18	6.385	1.276×10^{3}
#22	16.14	5.046×10^{4}
#26	40.81	1.996×10^{4}
#30	103.2	7.894×10^{5}

Fig. 6-3. Resistance and Cross-sectional Area of Several Sizes of Annealed Copper Wire

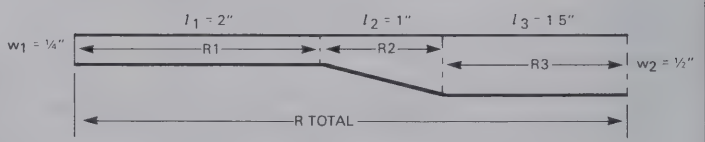


Fig. 6-4. Conductor of Uniform Thickness but Non-uniform Cross-section

The middle segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1} \ln\left(\frac{w_2}{w_1}\right) = 4 \ln 2 = 2.77 \text{ squares} \quad (6\text{-}5)$$

$$Total\ R = R_1 + R_2 + R_3 = \rho_S (S_1 + S_2 + S_3) = 7.51\ m\Omega$$

As another example, assume that a 1 oz. trace must carry a 200 mA current 6 inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\ \Omega$$

$$0.05 = \rho_S \frac{l}{w}$$

$$\frac{w}{l} = 20\ \rho_S$$

$$w = 120\ \rho_S = (120)\ 5.657 \times 10^{-4} = 67.9 \times 10^{-3} \quad (6\text{-}6)$$

$$\therefore \text{minimum trace width, } w = 68 \text{ mils}$$

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50 A current.

$$\rho_S = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square} \quad (6\text{-}7)$$

$$V = IR = (50)\ (3.364 \times 10^{-5})\ \frac{36}{1.25} = 0.0484 = 48.4\ mV$$

Sheet resistances for various copper thicknesses are listed in *Figure 6-5*. Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 6-6* and resistance per foot as a function of width is shown in *Figure 6-7*.

TEMPERATURE COEFFICIENT

The resistances in *Figures 6-3, 6-5,* and *6-7,* as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature T can be determined as follows.

$$R_T = R_{20°}\ [1 + 0.004\ (T - 20°)]$$

At 55°C:

$$R = R_{20°}\ [1 + 0.004\ (55° - 20°)] = 1.14\ R_{20°} \quad (6\text{-}8)$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 6-8* illustrates the ohmic heating effect of various current densities.[1]

Weight or Thickness	Sheet Resistance Ω per square	Thickness	Sheet Resistance Ω per square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

Fig. 6-5. Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	weight, %	in.
0.0007	0.0178	1/2	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 -0.0002
0.0028	0.0715	2	+10	+0.0007 -0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

Fig. 6-6. Thicknesses and Tolerances for Copper Cladding

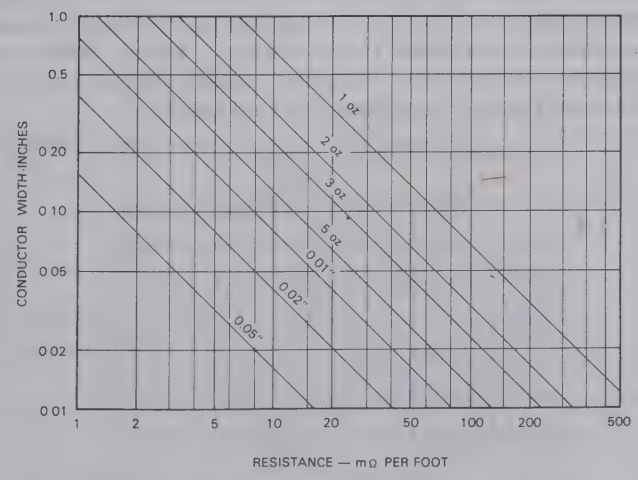


Fig. 6-7. Conductor Resistance Versus Thickness and Width

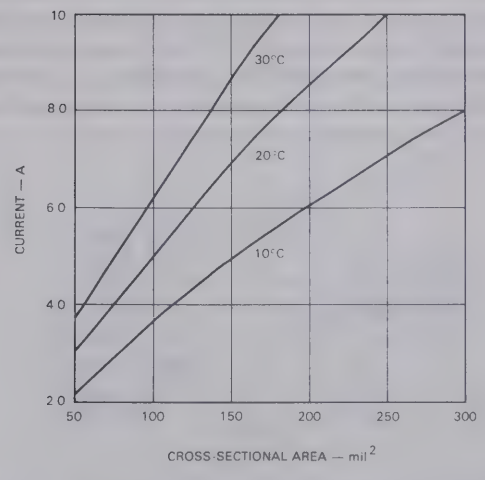


Fig. 6-8. Temperature Rise with Current Density in PC Board Traces

DISTRIBUTION IMPEDANCE

Power busses should have low ac impedance, as well as low dc resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 6-9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75 Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377}{\sqrt{\epsilon}} \frac{d}{h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar* or Teflon* dielectric ($\epsilon = 2.3$) two mils thick, impedance of the flat conductor pair is only 0.5 Ω. Power line impedance can also be reduced by periodically connecting RF type capacitors across the line; this effect is discussed in Chapter 4.

GROUND ON PC CARDS

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CC} leads of the IC packages, through the output transistors, then into the loads and the stray capacitances. Stray capacitances exist from an output to V_{EE}, to ground and to the terminations of other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every four to six IC packages. These capacitors should be ceramic, mica or other RF types in the 0.01 to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, a signal change into a 50 Ω line causes about 17 mA current change and, as this current change propagates along the signal trace, a current of –17 mA is advancing along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. When it is necessary to interrupt the ground plane to provide crossover links between V_{EE} distribution lines or signal traces on the other side of the board, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

BACKPLANE SIGNAL GROUND

A ground return path must be provided to control the impedance of single-ended point-to-point signal wiring between connectors in the backplane. If a motherboard is used as the backplane for a row of cards, one side of the motherboard can be a ground plane. Interconnect wires then exhibit an impedance which can be calculated from the wire-over-ground formula.

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \log \frac{4h}{d} \qquad (6\text{-}9)$$

where d is diameter, h is distance to ground, ϵ is dielectric constant.

For small insulated wire, the impedance ranges from about 75 Ω when lying flat against ground to about 150 Ω when spaced one diameter, including insulation, above ground. With one side of a motherboard committed to ground, the other side can be used to distribute timing signals and dc voltages.

When a motherboard is not practical, a ground screen can be used to establish the backplane signal wiring impedance. A screen is constructed by connecting the grounds of each card connector, as illustrated in *Figure 6-10*. Wires running over a ground screen exhibit an impedance in the range of 100 to 200 Ω, depending on distance from the screen, mesh size and the angular direction. The wires forming the screen provide a means for the signal return current to find a "piece-wise optimum" return path. Thus, the smaller the screen mesh, the more nearly it simulates a ground plane.

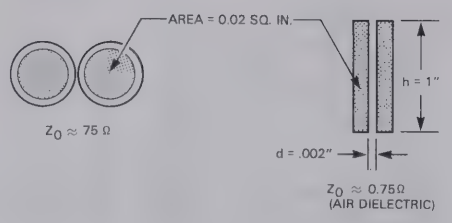


Fig. 6-9. Effect of Geometry on Power Bus Impedance

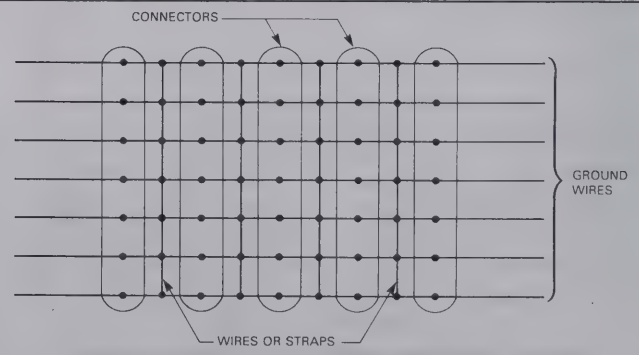


Fig. 6-10. Ground Screen

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company

TERMINATION SUPPLY V_{TT}

A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A –2 V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 6-11* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to –2 V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cycle values are useful in determining the current drain on the –2 V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

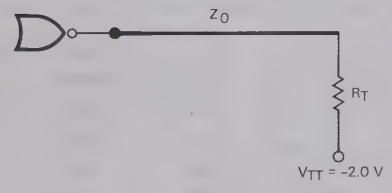
Regulation of the –2 V supply is not critical; a variation of ±5% causes a change in outut levels of ±12 mV for 50Ω terminations or ±7 mV for 100Ω terminations. If V_{TT} is distributed on a logic board by using etched traces, as opposed to a solid voltage plane, decoupling capacitors to ground should be used to reduce the effective dynamic impedance of the traces. The capacitors should be distributed in about the same pattern as the termination resistors, with 0.01 µF for every four terminations. A 1 to 10 µF decoupling capacitor to ground should be placed on the card near the point where the V_{TT} supply enters from the backplane.

V_{EE} SUPPLY

The value of the V_{EE} voltage is not critical for F95K or F10K ECL, since they operate successfully over the range –4.7 to –6.2 V; simple OR/NOR gate elements operate from –3.7 to –6.2 V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should use a 1 to 10 µF decoupling capacitor near the point where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than –5.2 V, the current drain varies as shown in *Figures 6-12* and *6-13* for SSI and MSI elements respectively. The figures also show the variations exhibited by conventional uncompensated 10,000 ECL.

If conventional 10,000 series ECL elements are randomly mixed with F10K circuits in the same system, the more restrictive V_{EE} requirements of the conventional 10,000 series must be observed. It is common practice to limit V_{EE} regulation to the nominal –5.2 V ±2% because the ac and dc parameters exhibit a sensitivity to V_{EE}. Circuit manufacturers recommend that for single-ended signal transmission between two circuits, their respective V_{EE} values should not differ by more than 100 mV, to limit noise margin loss to 30 mV. This loss occurs in the LOW state when the driver circuit V_{EE} is –5.1 V



R_T Ω	P_D (avg) mW		I_{avg} mA
	Resistor	IC Output	
50	13	14	14
62	11	12	11
75	9.1	9.5	9.3
90	7.9	8.2	8.1
100	7.1	7.3	7.3
150	5.0	4.9	5.0

Fig. 6-11. Average Current and Power Dissipation for Parallel Termination to -2 V

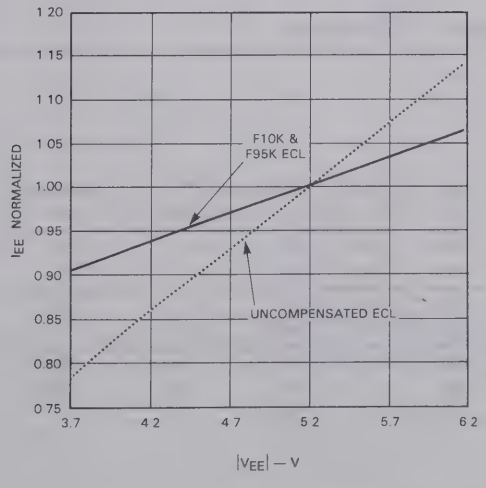


Fig. 6-12. Power Drain Current Versus Supply Voltage for ECL SSI

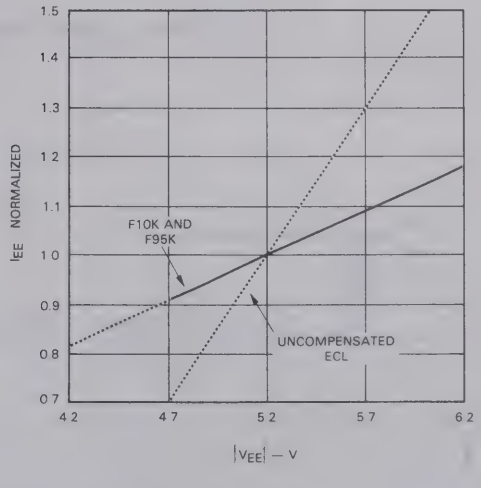


Fig. 6-13. Power Drain Current Versus Supply Voltage of ECL MSI

and the receiving circuit V_{EE} is –5.2 V. In this situation, substituting an F10K circuit for the driver reduces the noise margin loss from 30 to 3 mV.

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 6-14* for several representative values of equivalent resistance. The average values apply for 50% duty cycle; peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 6-11.* Average dissipation and I_{EE} current for several values of pull down resistance to V_{EE} are listed in *Figure 6-15.* The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from *Equation 5-12.* Peak current values are approximately 12% greater than average values.

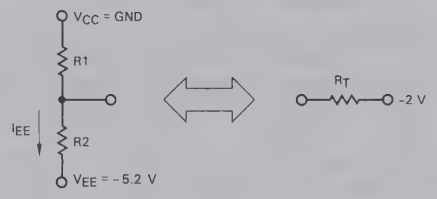
Figures 6-11, 14 and *15* show that the Thevenin equivalent parallel termination method leads to 10 times as much dissipation in the resistors as in the single resistor returned to –2 V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to –2 V.

In some applications, it may be advantageous to distribute power in unregulated form and use local regulators on the logic boards. Fairchild 3-terminal regulators (μA78N05, μA78N02) are designed specifically for ECL. The μA78N05 provides –5.2 V and the μA78N02 provides –2 V; both can operate from the same input voltage.

THERMAL CONSIDERATIONS

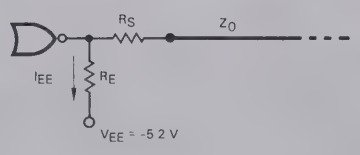
F95K and F10K circuits are specified over the standard industrial temperature range, 0°C to +75°C. Operation over a –30°C to +85°C range results in slight degradation of worst case parameter limits. System cooling requirements are based on three considerations. One is the need to minimize temperature gradients between circuits communicating in the single-ended mode. Another concerns controlling the temperature environment of each circuit to assure that the parameters stay within guaranteed limits. The thermal conditions must also insure that the maximum rated junction temperature is not exceeded.

Temperature gradients are of no practical concern with F95K circuits since they are temperature compensated; their output voltage levels and input thresholds change very little with temperature, as discussed in Chapter 2. With F10K and conventional 10,000 circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driver and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/°C of temperature gradient. When the driver circuit is at the higher temperature, the LOW state margin decreases by approximately 0.5 mV/°C of gradient. The system designer should consider noise margin loss, as well as the effects of ground potential differences



R_T Ω	R_1 Ω = 1.625 R_T	R_2 Ω = 2.6 R_T	P_D (avg) mW Resistors	I_{EE} (avg) mA
50	81	130	143	30
62	101	161	114	24
75	122	195	94	20
90	146	234	79	17
100	163	260	71	15
150	244	390	47	10

Fig. 6-14. Series Divider for Thevenin Equivalent Terminations



R_E Ω	Z_0 Ω	P_D (avg) mW R_E	P_D (avg) mW IC Output	I_{EE} (avg) mA
330	50	46	15	12
390	62	39	13	10
470	75	32	10	8.2
560	90	28	8.7	7.0
620	100	25	7.8	6.4
1K		16	4.8	4.0

Fig. 6-15. Average Power Dissipation and Current using Pull Down Resistor to V_{EE}

and V_{EE} gradients, when deciding whether to use single-ended wiring between two locations or to use differential wiring. Differential line receivers nullify the effects of temperature gradients, as well as V_{EE} gradients and ground voltage differences.

Each parameter limit on the F95K data sheets applies over the entire 0°C to 75°C temperature range, with either still or moving air. For F10K and conventional 10,000 series, parameter limits have different values for different ambient temperatures. Further, the specifications are based on a minimum air flow rate of 500 linear feet per minute. Thermal equilibrium must be established for incoming test results of F10K circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied. When an F10K circuit is operating with a cooling air temperature other than data sheet test temperatures, circuit parameter values can be estimated by interpolation. For example, if the cooling air temperature is +50°C, the circuit V_{OH} can be estimated by averaging the V_{OH} values for +25°C and +75°C.

The maximum rated junction temperature of F95K and F10K circuits is +150°C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance Θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the dissipation in the output transistors from *Figure 6-11* or *6-15*. The thermal resistance for the 16-lead ceramic DIP is shown in *Figure 6-16* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D\theta_{JA} \tag{6-10}$$

Conversely, when the maximum rated junction temperature (+150°C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

$$Maximum\ \theta_{JA} = \frac{(150^\circ - T_A)}{P_D} \tag{6-11}$$

For this value of Θ_{JA}, the minimum flow rate is determined from *Figure 6-16*.

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For instance, on a densely packed logic board in a horizonal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises, due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

REFERENCE

1. Harper, C.A., Editor, Handbook of Wiring, Cabling and Interconnecting for Electronics, McGraw-Hill, 1972.

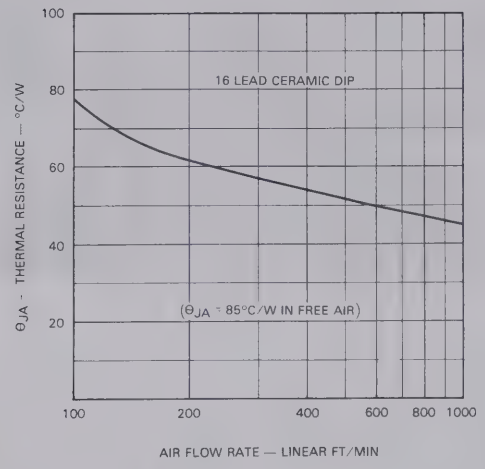


Fig. 6-16. Junction-to-Air Thermal Resistance Versus Air Flow Rate

ECL PRODUCT INFORMATION

DEFINITIONS OF SYMBOLS AND TERMS

The symbols and terms used in the data sheets have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits are referenced to an algebraic scale. The extremities of the scale are:

"A" the value closest to positive infinity.
"B" the value closest to negative infinity.

CURRENTS

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional current flow *out of* a device lead.

I_{EE} (Power Supply Current) — The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} (Input Current HIGH) — The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case dc input load that a device presents to a driving element.

I_{IL} (Input Current LOW) — The current flowing into a device lead with the specified V_{IL} applied to the input.

VOLTAGES

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage) — The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground) — This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CS} (Current Source Voltage) — The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage) — This potential is the system power supply voltage and it is the most negative potential in the system.

V_{IH} (Input Voltage HIGH) — The range of input voltages that represents a logic HIGH level in the system.

V_{IHA} — The most positive V_{IH}.

V_{IHB} — The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW) — The range of input voltages that represents a logic LOW level in the system.

V_{ILA} — The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

V_{ILB} — The most negative V_{IL}.

V_{OH} (Output Voltage HIGH) — The range of voltages at an output terminal with the specified output loading and with the inputs condition to establish a HIGH level at the output.

V_{OHA} — The most positive V_{OH} under the specified input and loading conditions.

V_{OHB} — The most negative V_{OH} under the specified input and loading conditions.

V_{OHC} — The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW) — The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

V_{OLA} — The most positive V_{OL} under the specified input and loading conditions.

V_{OLB} — The most negative V_{OL} under the specified input and loading conditions.

V_{OLC} — The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin) — Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and V_{IHB}.

V_{NL} (LOW Level Noise Margin) — Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between V_{ILA} and V_{OLC}.

AC SWITCHING PARAMETERS

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency) — The maximum repetition rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{AA} (Address Access Time) — 50% points of address input pulse to data output pulse.

t_{ACS} (Chip Select Access Time) — 50% points of select pulse to data output pulse/leading edges.

t_h (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{RCS} (Chip Select Recovery Time) — Data output pulse/ trailing edges.

t_s (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_{TLH} (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_w (Pulse Width) — The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_W (Write Pulse Width) — 50% points of write enable input pulse.

t_{WHA} (Address Hold Time) — 50% points of address pulse to trailing edge of write enable pulse.

t_{WHCS} (Chip Select Hold Time) — 50% points of trailing edges of chip select pulse to write enable pulse.

t_{WHD} (Data Hold Time After Write) — 50% points of trailing edges of data input pulse to write enable pulse.

t_{WR} (Write Recovery Time) — 50% points of trailing edges of write enable pulse to data output pulse.

t_{WS} (Write Disable Time) — 50% points of leading edges of write enable pulse to data output pulse.

t_{WSA} (Address Set-up Time) — 50% points of address pulse to leading edge of write enable pulse.

t_{WSCS} (Chip Select Set-up Time) — 50% points of leading edges of chip select pulse to write enable pulse.

t_{WSD} (Data Set-up Time Prior to Write) — 50% points of leading edges of data input pulse to write enable pulse.

LINEAR APPLICATION TERMS

BANDWIDTH — The frequency at which the gain is 3 dB below its low frequency value.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

COMMON MODE INPUT VOLTAGE RANGE — The permissible range of input bias voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other tied to V_{BB}.

OUTPUT RESISTANCE — The resistance seen looking into an output terminal.

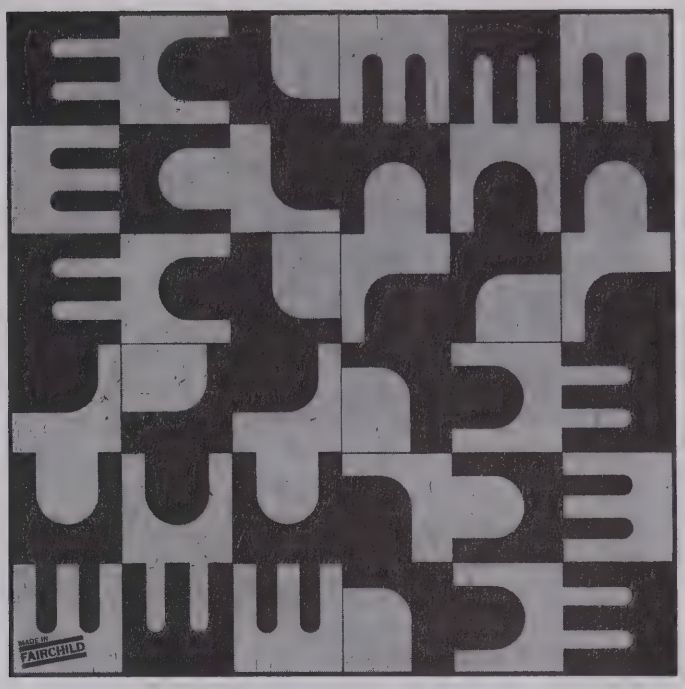
OUTPUT SOURCE CURRENT — Peak positive current available at an output.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. The output is loaded with 220 Ω to -5.2 V.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

VOLTAGE GAIN — The ratio of the change in the output voltage to the change in voltage between the input terminals producing it.

THE ECL HANDBOOK SECTION SELECTOR



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F95K Fully Compensated ECL Series 8

CHAPTER 7

F10000 4-Bit Shift Register
F10010 BCD Decade Counter
F10016 4-Bit Binary Counter
F10101 Quad OR/NOR Gate with Common Enable
F10102 Quad-2 NOR Gate
F10103 Quad-2 OR Gate
F10105 Triple 2-3-2-Input OR/NOR Gate
F10106 Triple 4-3-3-Input NOR Gate
F10107 Triple Exclusive OR/NOR Gate
F10109 Dual 4-5-Input OR/NOR Gate
F10110 Dual 3-Input/3-Output OR Gate
F10111 Dual 3-Input/3-Output NOR Gate
F10115 Quad Line Receiver
F10116 Triple Line Receiver
F10117 Dual 2-Wide 2-3-Input OR/AND, OR/AND/INVERT Gate
F10118 Dual 2-Wide 3-3-Input OR/AND Gate
F10119 4-Wide 4-3-3-3-Input OR/AND Gate
F10121 4-Wide 3-3-3-3-Input OR/AND, OR/AND/INVERT Gate
F10124 Quad TTL to ECL Translator
F10125 Quad ECL to TTL Translator
F10130 Dual D Latch
F10131 Dual D Flip-Flop
F10132 Dual Multiplexer/Latch
F10133 Quad Latch
F10134 Dual Multiplexer/Latch
F10160 12-Bit Parity Checker/Generator
F10161 1-of-8 Decoder (LOW)
F10162 1-of-8 Decoder (HIGH)
F10164 8-Input Multiplexer
F10170 11-Input Parity Checker/Generator
F10171 Dual 1-of-4 Decoder/Demultiplexer (LOW)
F10172 Dual 1-of-4 Decoder/Demultiplexer (HIGH)
F10173 Quad Multiplexer/Latch
F10174 Dual Multiplexer
F10175 Quint Latch
F10179 Carry Lookahead Generator
F10405 128 x 1-Bit Fully Decoded RAM
F10410 256 x 1-Bit Fully Decoded RAM
F10415 1024 x 1-Bit Fully Decoded RAM

F10K VOLTAGE COMPENSATED ECL SERIES

GENERAL DESCRIPTION — Fairchild F10K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic elements intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

F10,000 ECL is designed to be fully compatible with conventional 10,000 ECL and has the same part numbers, functions, pinouts, temperature behavior, test methods, propagation delay limits and signal voltages.

F10K circuits employ Emitter Coupled Logic to achieve typical power levels of 25 mW/gate. The nominal power supply is specified as V_{EE} equal to –5.2 V. All devices, however, may be operated over V_{EE} ranges of –4.7 to –6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a V_{EE} range of –3.5 to –6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

In accordance with standard IC practice, F10K devices are specified over 0°C to +75°C temperature range. However, limits ensure that the F10K series is fully compatible with other 10,000 devices specified over a –30°C to +85°C ambient temperature range.

High input impedance (typically 50 kΩ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

- **Very high speed . . . typically 2 ns per gate.**
- **Low power dissipation . . . typically 25 mW per gate.**
- **Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.**
- **Internal 50 kΩ (nominal) input pull down resistors . . . unused inputs may be left open.**
- **Open emitter-follower outputs drive terminated lines.**
- **Separate V_{CC} leads eliminate noise coupling.**
- **Single V_{EE} power supply . . . –4.7 to –6.2 V.**
- **Wired-OR capability.**
- **Complementary, simultaneous outputs.**
- **Fully compatible with other 10,000 series ECL.**

RECOMMENDED OPERATING AND TEST CONDITIONS — The Fairchild F10K series is designed to operate in a system whose ambient temperature is controlled by moving air or equivalent means. The ambient temperature may be any value between 0°C and +75°C, but the temperature gradient between the devices must be at a minimum to conserve noise immunity. The Fairchild F10K devices are designed to meet the specified dc characteristics when a thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to –2.0 V.

The Fairchild F10K series operates with a system power supply V_{EE} between –4.7 and –6.2 V. Detailed test specifications are for nominal V_{EE} = –5.2 V.

ABSOLUTE MAXIMUM RATINGS

(Non-operating, above which useful life may be impaired)

Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–8 V
Input Voltage	Gnd to V_{EE}
Output Current	–50 mA

FUNCTIONAL DESCRIPTION

F10K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1.*

If the input voltages are more negative than V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than V_{BB}, Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

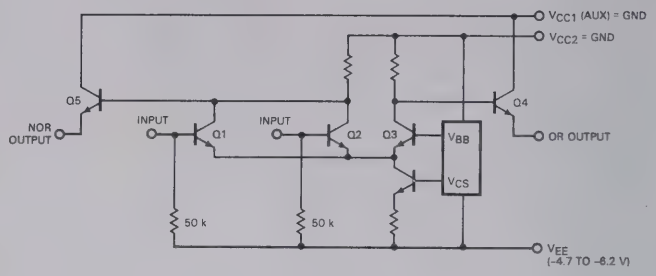


Fig. 1.

TYPICAL ECL TRANSFER CHARACTERISTICS WITH SPECIFICATION POINTS

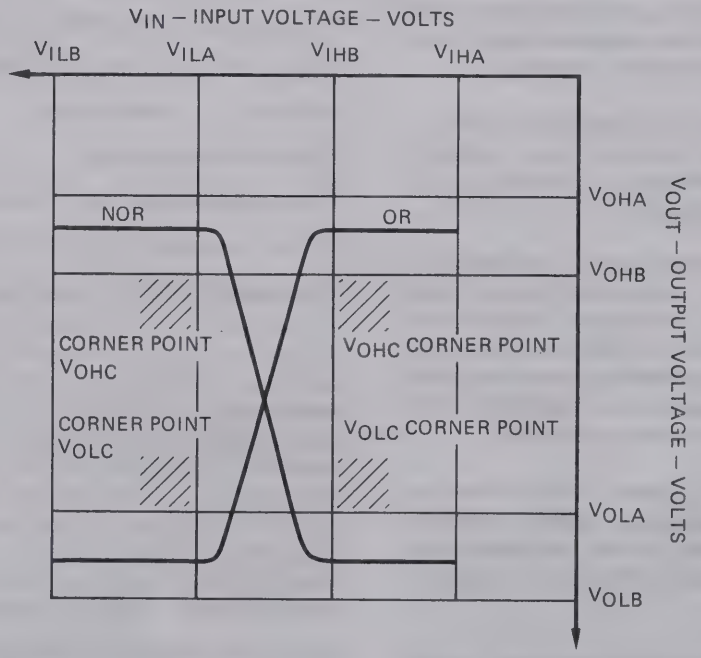
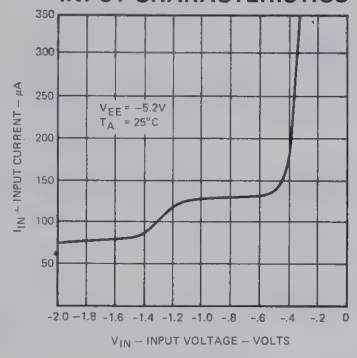


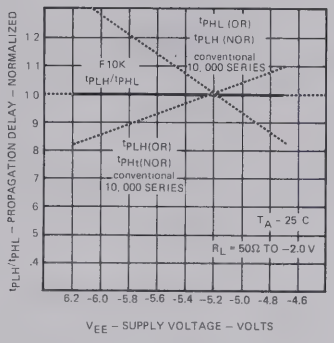
Fig. 2.

TYPICAL F10K SERIES CHARACTERISTICS

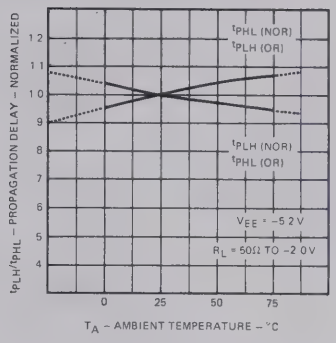
INPUT CHARACTERISTICS



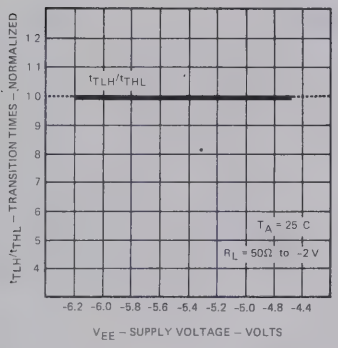
PROPAGATION DELAY VARIATION VERSUS SUPPLY VOLTAGE



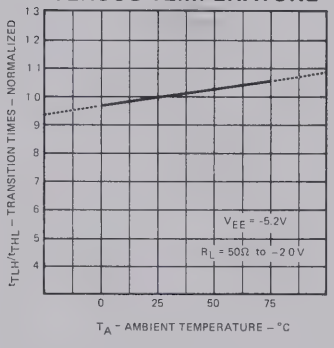
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE



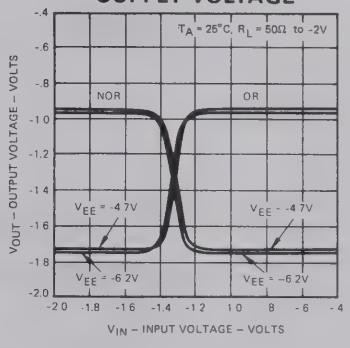
OUTPUT TRANSITION TIME VARIATION VERSUS SUPPLY VOLTAGE



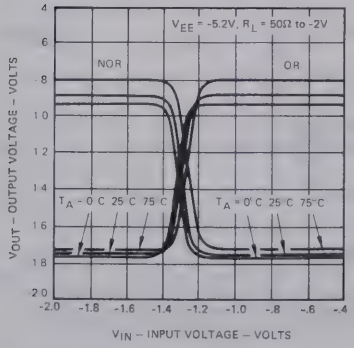
OUTPUT TRANSITION TIME VERSUS TEMPERATURE



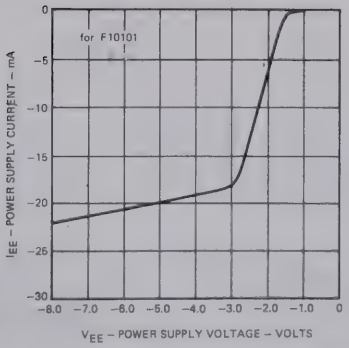
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



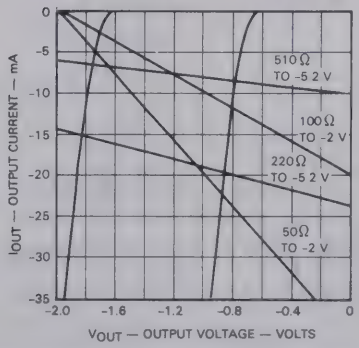
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



CHANGE IN POWER SUPPLY CURRENT WITH RESPECT TO CHANGES IN POWER SUPPLY VOLTAGE

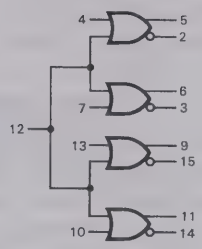


OUTPUT CHARACTERISTICS VERSUS TYPICAL OUTPUT TERMINATION SCHEMES

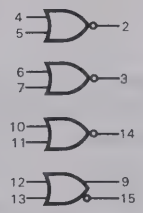


LOGIC DIAGRAMS $V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8$

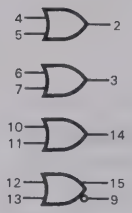
F10101



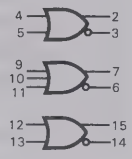
F10102



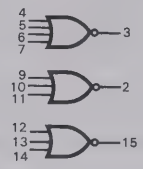
F10103



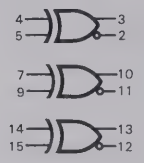
F10105



F10106



F10107

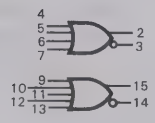


Logic Equation

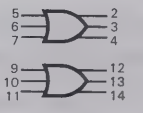
$2 = 4 \cdot \overline{5} + \overline{4} \cdot 5$

$3 = 4 \cdot 5 + \overline{4} \cdot \overline{5}$

F10109

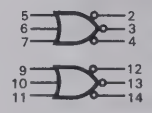


F10110



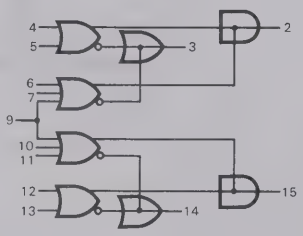
NOTE: $V_{CC1} = 1$
$V_{CC2} = 15$

F10111



NOTE: $V_{CC1} = 1$
$V_{CC2} = 15$

F10117

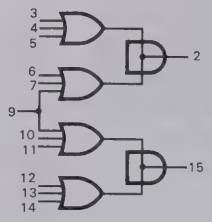


Logic Equation

$2 = (4 + 5)(6 + 7 + 9)$

$3 = \overline{(4 + 5)(6 + 7 + 9)}$

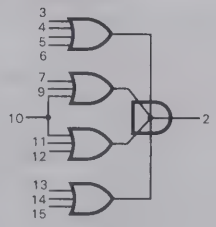
F10118



Logic Equation

$2 = (3 + 4 + 5)(6 + 7 + 9)$

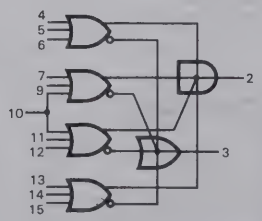
F10119



Logic Equation

$2 = (3 + 4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)$

F10121



Logic Equation

$2 = \overline{(4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)}$

$3 = (4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)$

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND **F10101 • F10102 • F10103 • F10105 • F10106 F10107 • F10109 • F10110 • F10111**

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	-1000		-840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Logic Function
		-960		-810		25°C	
		-900		-720		75°C	
V_{OL}	Output Voltage LOW	-1870		-1665	mV	0°C	
		-1850		-1650		25°C	
		-1830		-1625		75°C	
V_{OHC}	Output Voltage HIGH	-1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function; Loading is 50Ω to -2.0 V
		-980				25°C	
		-920				75°C	
V_{OLC}	Output Voltage LOW			-1645	mV	0°C	
				-1630		25°C	
				-1605		75°C	
V_{IH}	Input Voltage HIGH	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		-1105		-810		25°C	
		-1045		-720		75°C	
V_{IL}	Input Voltage LOW	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		-1850		-1475		25°C	
		-1830		-1450		75°C	
I_{IH}	Input Current HIGH			265	μA	25°C	$V_{IN} = V_{IHA}$
	F10101 Lead 12			550			
	F10107 Leads 5,7,15			220			
	F10110 All Inputs			435			
	F10111 All Inputs			435			
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current F10101	-26	-20		mA	25°C	Inputs and Outputs Open
	F10102	-26	-20				
	F10103	-26	-20				
	F10105	-21	-15				
	F10106	-21	-15				
	F10107	-28	-22				
	F10109	-14	-10				
	F10110	-38	-28				
	F10111	-38	-28				

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C **F10101 • F10102 • F10103 • F10105 • F10106 • F10109**

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	2.0	2.9	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	2.0	2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.3	ns	

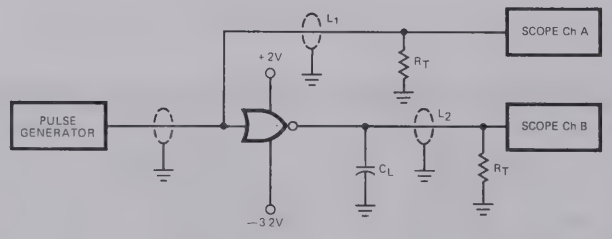
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C **F10107**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.1	2.4	3.7	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.1	2.4	3.7	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.5	ns	

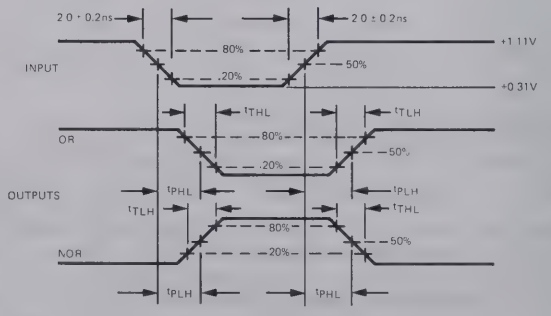
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C **F10110 • F10111**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.4	2.4	3.5	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.4	2.4	3.5	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

Fig 1

DC CHARACTERISTIC: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH OR-Tie Outputs	-1000 -960 -900		-740 -700 -610	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per logic function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW OR-Tie Outputs	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OH}	Output Voltage HIGH AND-Tie Outputs	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C		
V_{OL}	Output Voltage LOW AND-Tie Outputs	-1995 -1990 -1930		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per logic function	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH F10117 & F10118 Lead 9 F10119 & F10121 Lead 10			265 370 370	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-26	-20		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTIC: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.4	2.3	3.4 3.7(10117)	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.4	2.3	3.4 3.7(10117)	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	4.0	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	4.0	ns	

F10000

4-BIT SHIFT REGISTER

GENERAL DESCRIPTION — The F10000 is a 4-Bit Parallel/Serial In, Parallel/Serial Out Shift Register. High Speed ECL technology permits storage, shifting, counting and serial code conversion at rates in excess of 200 MHz.

Features include assertion outputs for each stage, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

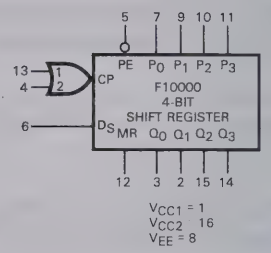
The F10000 incorporates a unique voltage compensation network which ensures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of power supply voltage.

- **HIGH SPEED . . . 200 MHz TYPICAL SHIFT FREQUENCY**
- **D TYPE INPUTS SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **TERMINATED LINE DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} LEADS ELIMINATE NOISE COUPLING**
- **50 kΩ INPUT PULL DOWNS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **SINGLE V_{EE} POWER SUPPLY . . . -4.7 V TO -6.2 V**
- **NOISE MARGINS INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS**

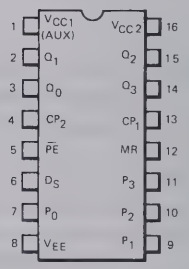
LEAD NAMES

P_n	Parallel Data Inputs
$\overline{PE}$	Parallel Enable (Active LOW)
CP_n	Clock In, Shifts on Positive Transition
MR	Asynchronous Master Reset — Active HIGH
D_S	Data Input, Serial
Q_n	Register Outputs

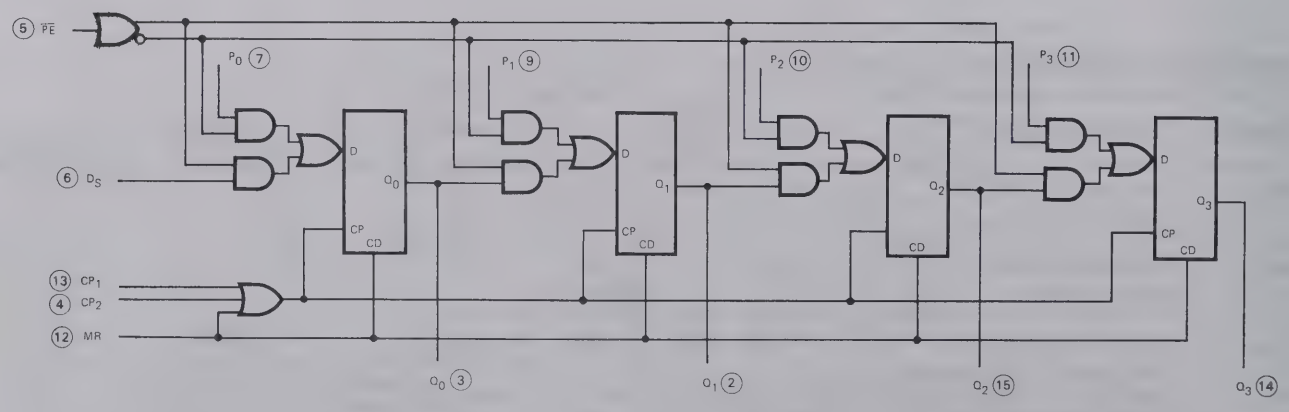
LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



○ = LEAD NUMBERS

Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10000 is a high speed 4-Bit Shift Register. It consists of four master/slave flip-flops and four 2-input multiplexers interconnected so as to permit loading of the masters from either a preceding slave output (Q_{n-1}) or an external (P_n) input. The function desired is selected by the Parallel Enable ($\overline{PE}$) input.

The masters are loaded during the LOW period of the clock ($CP_{1,2}$). As the clock changes from LOW to HIGH, the masters are inhibited from change followed by the enabling of the data path from master to slave. This data is then presented at the outputs (Q_n). While the clock is HIGH, the masters are inhibited from change and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited. This is followed by the enabling of the masters for the acceptance of data from the parallel or serial logic inputs.

As the two clock inputs are ORed together, both must be LOW for the masters to accept new data. If either is raised to a HIGH, the register is clocked.

A HIGH on one Clock input can prevent the register from shifting, providing a hold condition. To prevent false triggering, this input must change from LOW to HIGH while the clock is HIGH.

The Master Reset (MR) function is asynchronous. When held HIGH, it overrides all other commands and forces all outputs (Q_n) LOW.

TRUTH TABLES

MODE SELECT

MR	$\overline{PE}$	CP_1	CP_2	MODE
H	X	X	X	RESET (ALL OUTPUTS LOW)
L	L	L	⎍	PARALLEL LOAD
L	L	⎍	L	PARALLEL LOAD
L	H	L	⎍	SHIFT RIGHT (SERIAL LOAD)
L	H	⎍	L	SHIFT RIGHT (SERIAL LOAD)
L	X	H	X	HOLD
L	X	X	H	HOLD

SERIAL LOAD

D_S	$Q_{0(t+1)}$
H	H
L	L

PARALLEL LOAD

P_n	$Q_{n(t+1)}$
H	H
L	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

⎍ = Clock Pulse (LOW to HIGH)

(t+1) = Time after positive going clock transition

DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

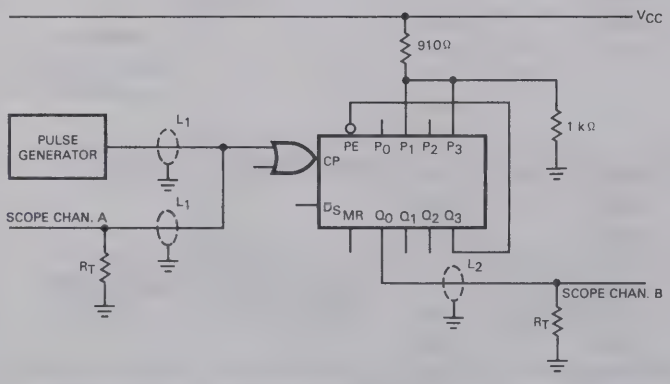
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH MR (Lead 12)			260 700	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–85	–66		mA	25°C	Outputs Open, Lead 4 or 13 Tied to V_{IH}	

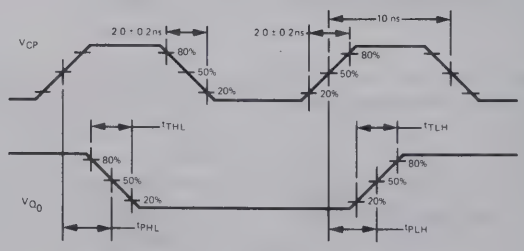
7

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Shift Right Frequency	150	200		MHz	See Figure 3
t_{PLH}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	See Figure 1
t_{PHL}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		2.5		ns	See Figure 2
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.0	3.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.0	3.5	ns	
t_w	Clock Pulse Width		2.5		ns	See Figure 3
t_w	MR Pulse Width		3.5		ns	
t_s	Set-Up Time Prior to Clock D_S to CP, P_n to CP	1.5	0.5		ns	
t_h	Hold Time After Clock D_S to CP, P_n to CP	1.0	–0.5		ns	
t_s	Set-Up Time Prior to Clock PE to CP	5.4	3.2		ns	
t_h	Hold Time After Clock PE to CP	0	–3.2		ns	

SWITCHING CIRCUITS AND WAVEFORMS

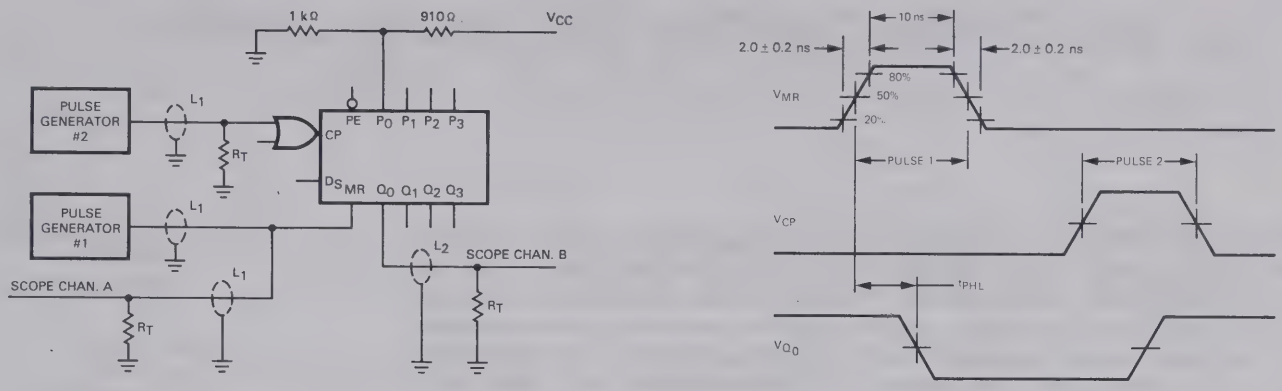




$L_1 = L_2 = 50\Omega$ impedence lines
V_{CC} = +2.0 V, Lead 1 and 16
V_{EE} = –3.2 V, Lead 8
$R_T = 50\Omega$ termination of scope
f = 10 MHz
Pulse Width = 10 ns

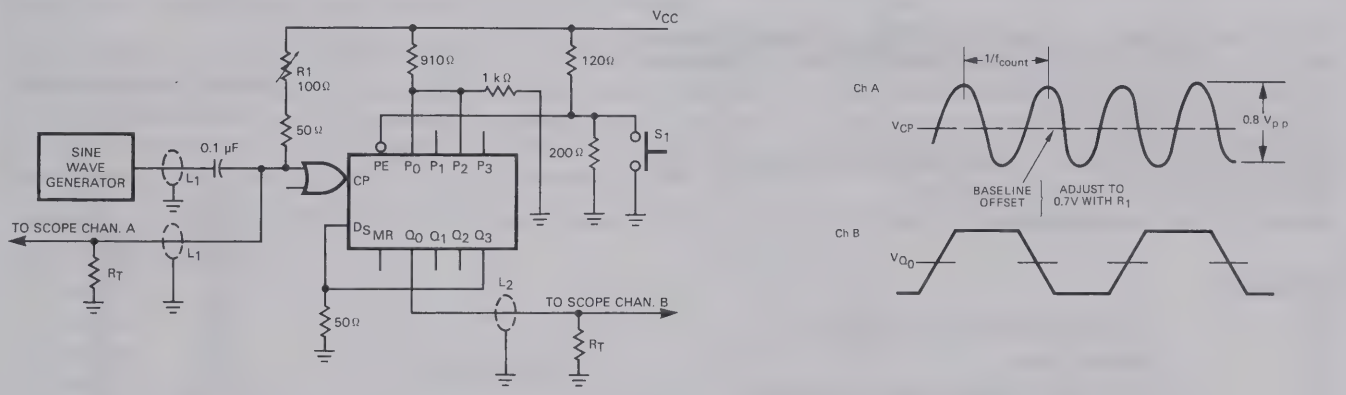
Fig. 1. Clock to Output, Output Transition Time

SWITCHING CIRCUIT AND WAVEFORMS (Cont'd)



$L_1 = L_2 = 50\Omega$ impedance lines.
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\Omega$ Termination of Scope
f = 10 MHz
Pulse 2 ≃ Pulse 1

Fig. 2. Master Reset to Output



$L_1 = L_2 = 50\Omega$ impedance lines
$V_{CC1} = V_{CC2} = +2.0$ V
$R_T = 50\Omega$ termination of scope
$f = f_{MAX}$
Load the register by closing S_1

Fig. 3. Shift Frequency

F10010 • F10016

BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F10010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F10016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 10K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

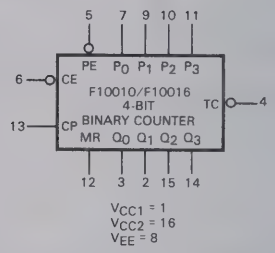
Both devices are packaged in hermetic ceramic 16-lead Dual In-Line packages and are specified for operation over the temperature range 0°C to 75°C.

- **HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY**
- **INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION**
- **ASYNCHRONOUS MASTER RESET**
- **50 Ω DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} LEADS — ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL DOWNS**
- **SINGLE -5.2 V POWER SUPPLY**

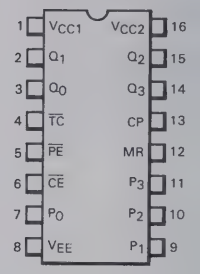
LEAD NAMES

$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (10010, LOW at HLLH; 10016 LOW at HHHH)
Q_n	Counter Outputs

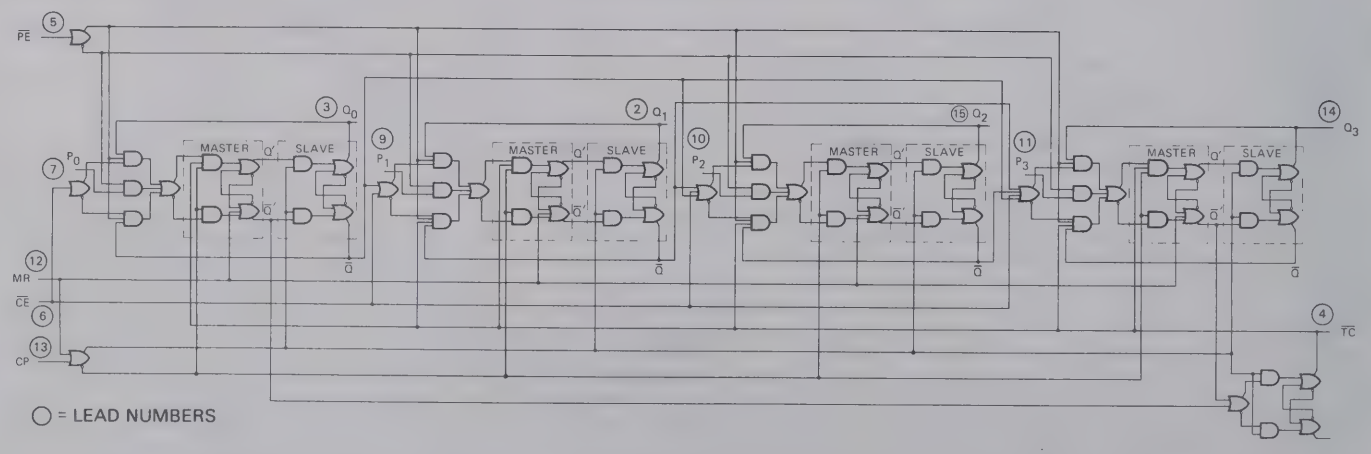
LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)

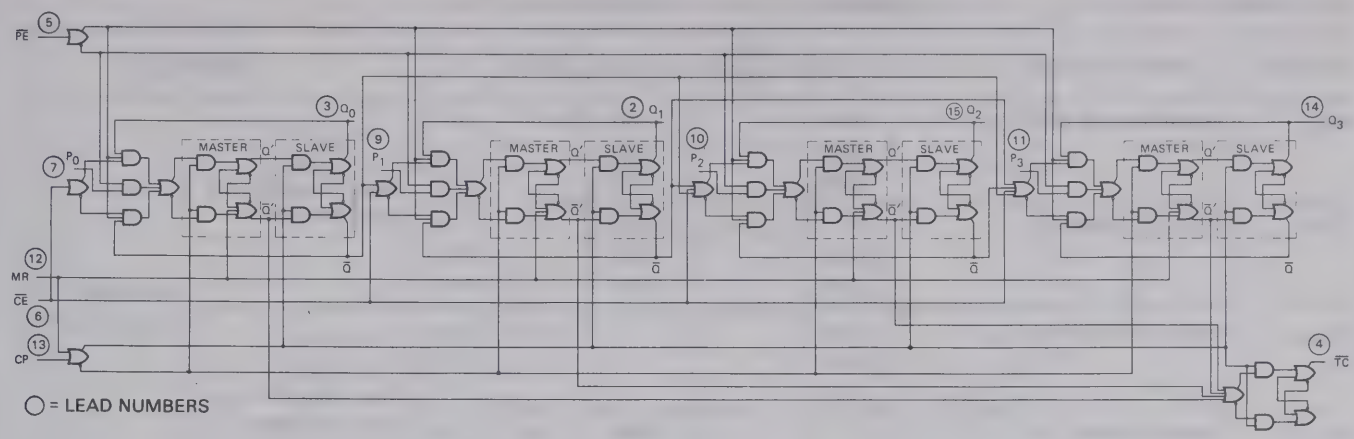


LOGIC DIAGRAM F10010



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC DIAGRAM F10016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10010 is a high speed BCD Decade Counter and the F10016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 10010 and at count 15 (HHHH) on the 10016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

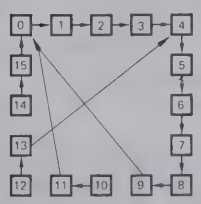
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	⎍	Load Parallel (P_n to Q_n)
H	L	L	⎍	Load Parallel (P_n to Q_n)
L	H	L	⎍	Count
H	H	L	⎍	Hold
X	X	L	⎏	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

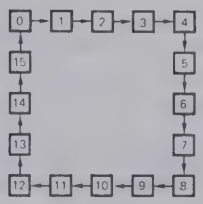
L = LOW
H = HIGH Voltage Level
X = Don't Care
⎍ = Clock Pulse (LOW to HIGH)
⎏ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F10010



F10016



NOTE: The 10010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15 , it will return to its normal sequence within two clock pulses.

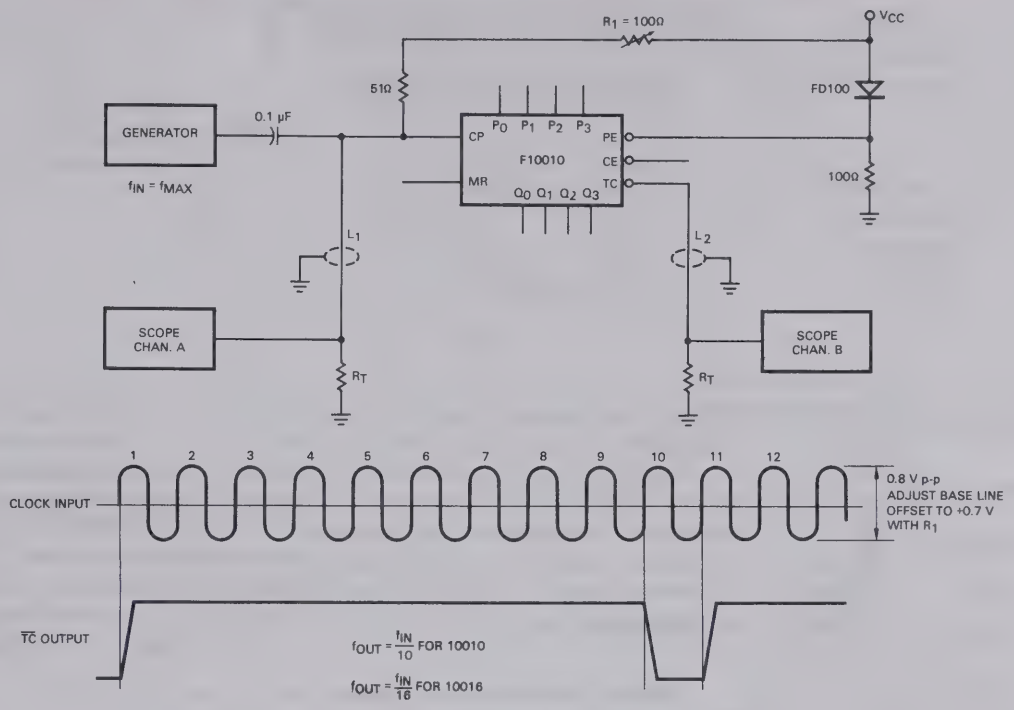
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH MR (Lead 12)			265 700	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-115	-80		mA	25°C	Outputs Open, Lead 12 Tied to V_{IH}	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_h	Hold Time After Clock P_n to CP	1.0			ns	
t_s	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
t_h	Hold Time After Clock PE or CE to CP	0.5			ns	

SWITCHING CIRCUITS AND WAVEFORMS

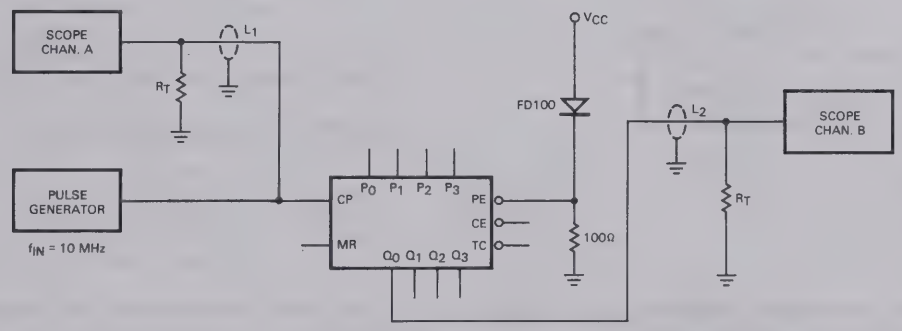


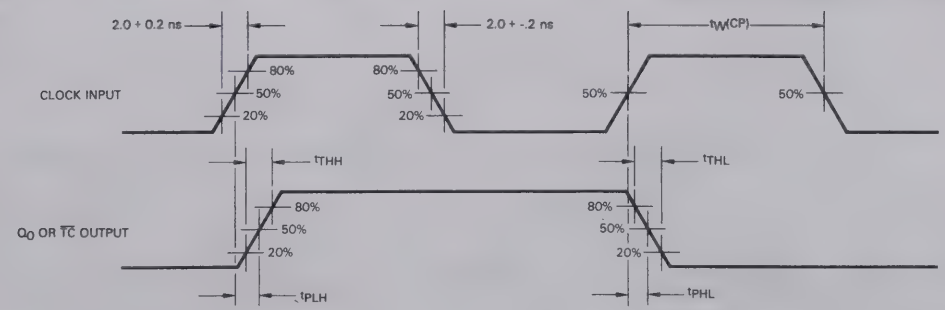
1 2 3 4 5 6 7 8 9 10 11 12
CLOCK INPUT
0.8 V p-p
ADJUST BASE LINE
OFFSET TO +0.7 V
WITH R1
TC OUTPUT
fOUT = fIN/10 FOR 10010
fOUT = fIN/16 FOR 10016

L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency



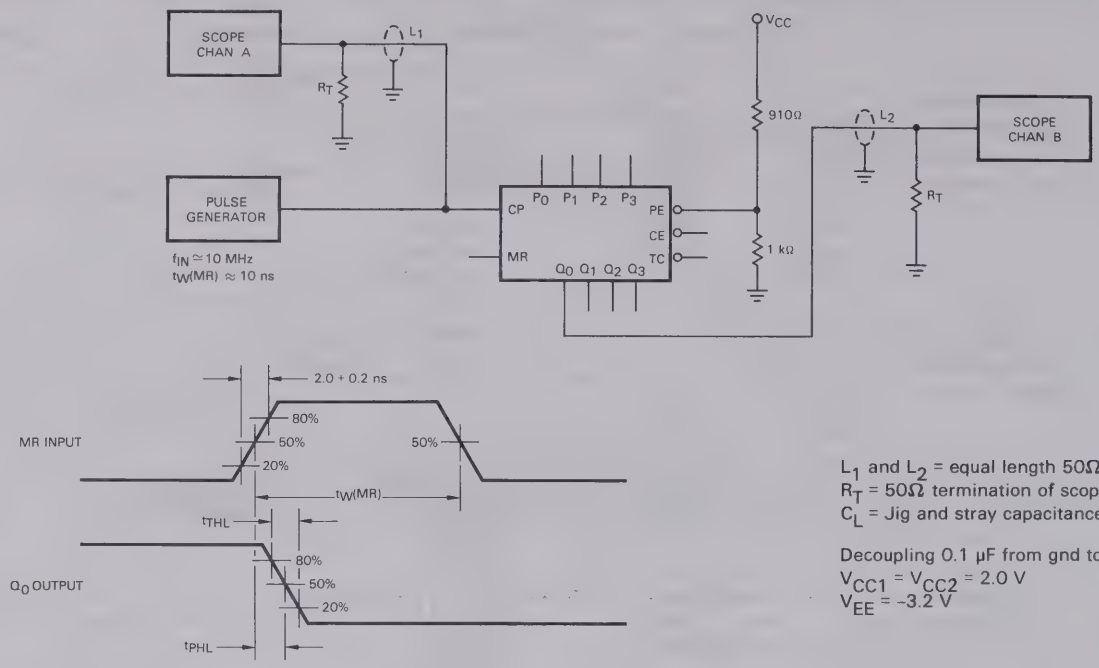


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Clock to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd)

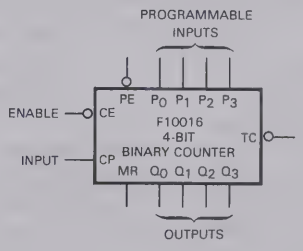


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

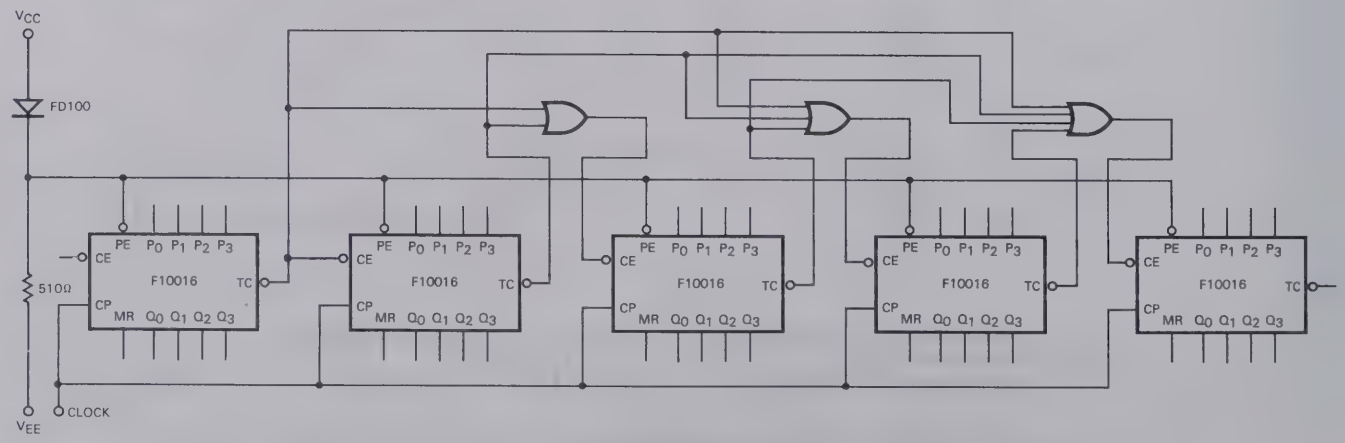
Fig. 3. Master Reset to Output

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F10016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.

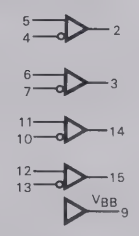


CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION

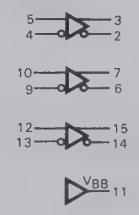
F10115 · F10116
LINE RECEIVERS

DESCRIPTION — The F10115 and F10116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide improved common mode rejection. The F10115 is a quad line receiver with single ended outputs. The F10116 is a triple line receiver with complementary outputs. The devices are voltage compensated and are fully compatible with other 10,000 series devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high speed comparators, oscillators, or broadband amplifiers.

LOGIC DIAGRAM



F10115



F10116

TRUTH TABLES

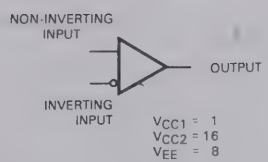
F10115 Quad Line Receiver

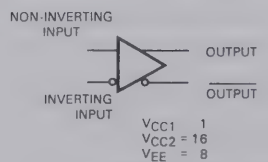
NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	H	L
V_{BB}	L	H

F10116 Triple Differential Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L

FUNCTIONS





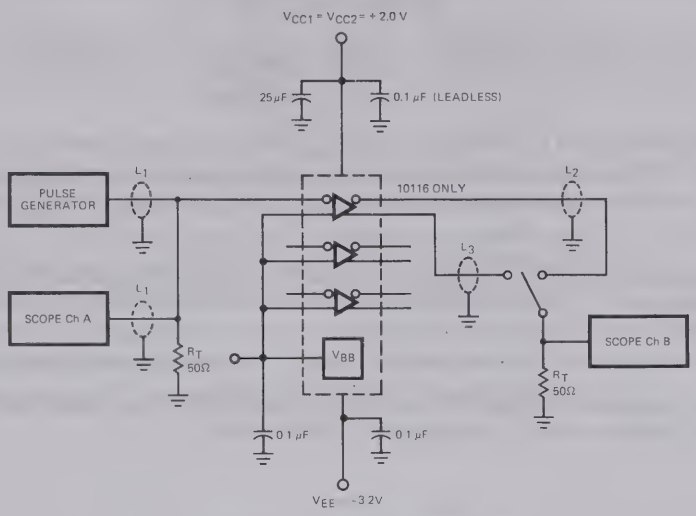
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

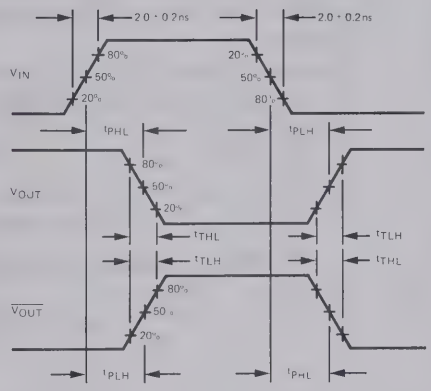
SYMBOL	CHARACTERISTIC		LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH		-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW		-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH		-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW				-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH		-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW		-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH				95	µA	25°C	$V_{IN} = V_{IHA}$	
I_{CBO}	Input Collector – Base Leakage Current		-1.0			µA	25°C	V_{IN} = -5.2 V	
I_{EE}	Power Supply Current	F10115	-26	-18		mA	25°C	Leads 4,7,10,13 = V_{ILB}, Leads 5,6,11,12 = V_{BB}	
		F10116	-21	-14		mA	25°C	Leads 4,9,12 = V_{ILB}, Leads 5,10,13 = V_{BB}	
V_{BB}	Reference Voltage		-1380 -1350 -1305		-1255 -1230 -1165	mV	0°C 25°C 75°C	F10115, Connect Leads 5,6,11,12 to Lead 9 F10116, Connect Leads 5,10,13 to Lead 11	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.0		2.9	ns	See Figure 1.
t_{PHL}	Propagation Delay, HIGH to LOW	1.0		2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





Unused outputs connect to a 50Ω resistor to ground.

One input from each gate must be tied to V_{BB} during testing.

L_1, L_2, and L_3 = equal length 50Ω impedance lines.

R_T = 50Ω termination of scope

Fig. 1

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor V_T may be calculated as follows:

$$V_T = \frac{(V_{EE} - V_{OH})\, R_T}{R_E + R_T + R_{LINE}}$$

Where V_{OH} is the output voltage HIGH of the driving gate, R_{LINE} is the resistance and R_T is the terminating resistor. With typical values, V_T is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between -0.55 and -3 V.

Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

TWISTED-PAIR CONNECTIONS

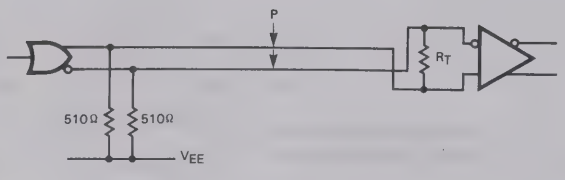


Fig. 2. Differential Transmission and Reception

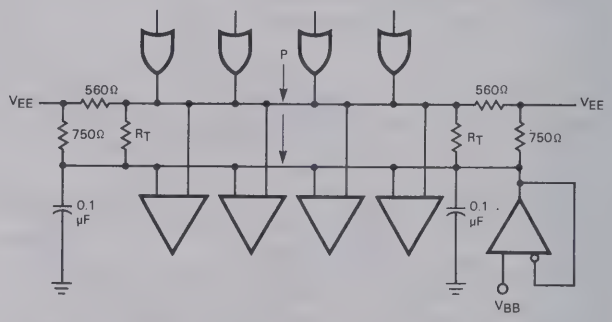


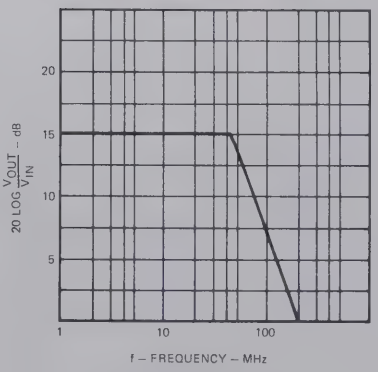
Fig. 3. Backplane Data Bus

PARAMETERS FOR LINEAR APPLICATIONS

V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

PARAMETER	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current		2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	-3.0		-0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		Vpp
Output Source Current			50	mA
Output Resistance		9		Ω

TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY

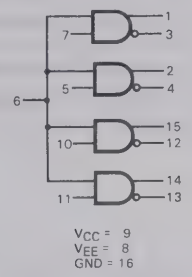


F10124
QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F10124 is a Quad Translator, designed to convert TTL logic levels to 10K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F10124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



Logic Equations $2 = 5 \bullet 6$, $4 = \overline{5 \bullet 6}$

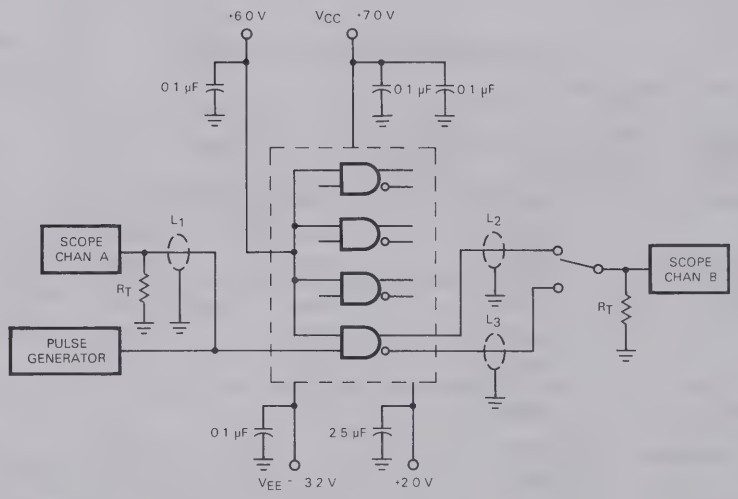
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = +5.0 V

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	V_{IN} = +4.0 V or +0.4 V per Logic Function	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	+1.9 +1.8 +1.8		5.0 5.0 5.0	V	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	0 0 0		+1.1 +1.1 +0.95	V	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
V_{CD}	Clamp Input Voltage	–1.5			V	25°C	I_{IN} = –10 mA	
V_{BD}	Input Breakdown Voltage	+5.5			V	25°C	I_{IN} = +1.0 mA, Other Inputs V_{IN} = GND	
I_{IH}	Input Current HIGH			50	µA	25°C	V_{IN} = +2.4 V, E_C V_{IN} = +0.4 V	
I_{IHX}	Input Current HIGH E_C			200	µA	25°C	E_C V_{IN} = +2.4 V, All Other Inputs V_{IN} = +0.4 V	
I_{ILX}	Input Current LOW E_C	–12.8			mA	25°C	E_C V_{IN} = +0.4 V, All Other Inputs V_{IN} = +4.0 V	
I_{IL}	Input Current LOW	–3.2			mA	25°C	V_{IN} = +0.4 V, E_C V_{IN} = +4.0 V	
I_{EE}	Power Supply Current	–34	–26		mA	25°C	Inputs and Outputs Open	
I_{CCH}	Power Supply Current		+13	+16	mA	25°C	All Inputs V_{IN} = +4.0 V	
I_{CCL}	Power Supply Current		+18	+25	mA	25°C	All Inputs V_{IN} = GND	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = +5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	3.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	3.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.9	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS



NOTES:

Connect unused outputs through 50Ω resistor to ground.
L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines.
R_T equals 50 Ω termination of scope

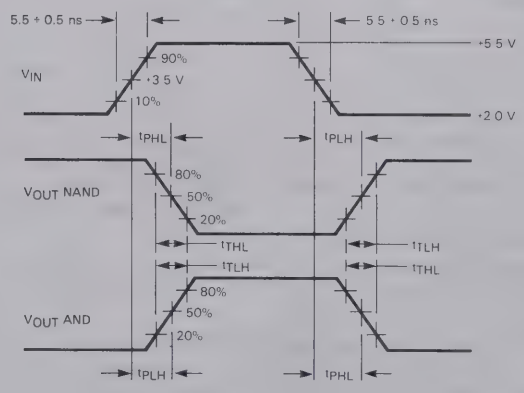


Fig. 1

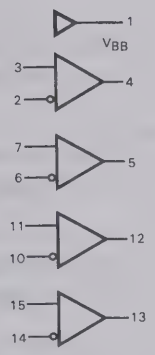
F10125

QUAD ECL TO TTL TRANSLATOR

DESCRIPTION — The F10125 is a Quad Translator for converting F10K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential line receiver. An internal reference voltage generator provides V_{BB} on lead 1 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go LOW when the inputs are left unconnected, have a fan out of 10 Schottky TTL loads.

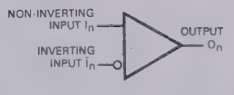
When used in the differential mode, the inputs have a common mode rejection of +1 V — making this device tolerant of ground offsets and transients between the signal source and the translator.

LOGIC DIAGRAM



V_{CC} = 9
V_{EE} = 8
GND = 16

FUNCTION



TRUTH TABLE

INPUTS		OUTPUT
Non-Inverting I_n	Inverting $\overline{I}_n$	O_n
L	H	L
H	L	H
L	L	*
H	H	*
OPEN	OPEN	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

*Undetermined

DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

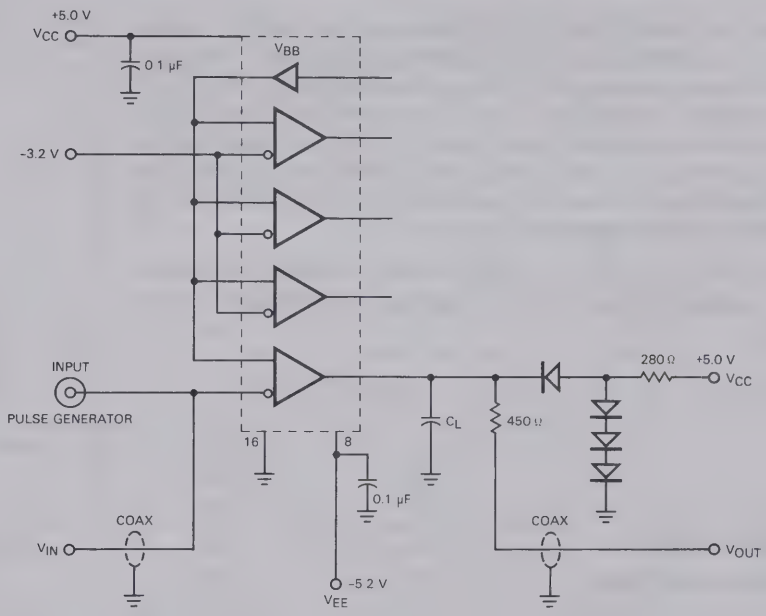
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is –2.0 mA V_{OH} +20 mA V_{OL}
V_{OL}	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C		
V_{OHC}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.160 +0.190 +0.280	V	0°C 25°C 75°C		
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	–0.870 –0.850 –0.830			V	0°C 25°C 75°C		
V_{IHL}	Common Mode Rejection Input Voltage HIGH –1.0 V			–1.840 –1.810 –1.720	V	0°C 25°C 75°C		
V_{ILL}	Common Mode Rejection Input Voltage LOW –1.0 V	–2.870 –2.850 –2.830			V	0°C 25°C 75°C		
V_{BB}	Reference Voltage	–1380 –1350 –1305		–1250 –1230 –1165	mV	0°C 25°C 75°C	$V_{IN} = V_{ILB}$	
I_{CBO}	Input Leakage Current	–1.0			µA	25°C	$V_{IN} = V_{EE}$ Note 1	
I_{IH}	Input Current HIGH			115	µA	25°C	$V_{IN} = V_{IHA}$ Note 1	
I_{OS}	Short Circuit Current	–100		–40	mA	25°C	V_{IN} = GND Note 2	
I_{EE}	Negative Power Supply	–40			mA	25°C	Inputs and Outputs Open	
I_{CCH}	Positive Power Supply			52	mA	25°C	$V_{IN} = V_{IHA}$ Note 3	
I_{CCL}	Positive Power Supply			39	mA	25°C	$V_{IN} = V_{ILB}$ Note 3	

NOTES:
1. Complementary Input = V_{BB}
2. One Output at a Time
3. Lead 2, 6, 10, 14 = V_{IN};
   Lead 3, 7, 11, 15 = Lead 1 (V_{BB})

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0		6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0		6.0	ns	
t_{TLH}	Output Transition Time 1.0 V to 2.0 V			3.3	ns	
t_{THL}	Output Transition Time 2.0 V to 1.0 V			3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



50Ω termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be <1/4 inch from TP_{IN} to input lead and TP_{OUT} to output lead.

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Lead 1) during testing.

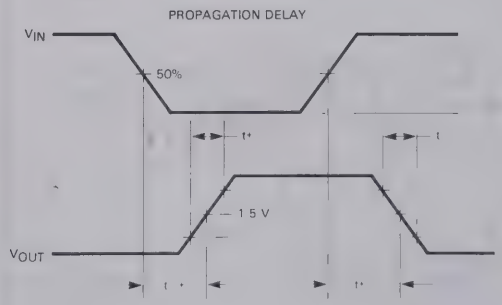


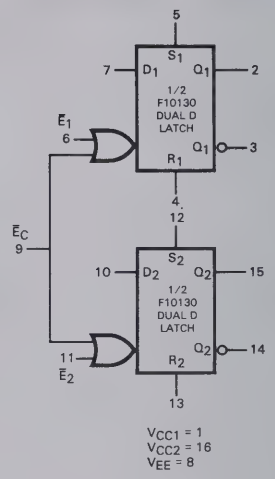
Fig. 1

F10130
DUAL D LATCH

DESCRIPTION — The F10130 contains a pair of D type latches with a Common Enable ($\overline{E}_C$) input. Each latch has its own Enable ($\overline{E}_n$), Set (S) and Reset (R) inputs. For each latch, the data present on the D input appears on the Q output when both $\overline{E}_n$ and $\overline{E}_C$ are LOW, as indicated in the truth table. As long as $\overline{E}_n$ and $\overline{E}_C$ remain LOW, the Q output follows the D input signal each time it changes. When either $\overline{E}_n$ or $\overline{E}_C$ (or both) go HIGH, the latch no longer responds to changes on the D input, but retains the last valid data present at D before $\overline{E}_n$ or $\overline{E}_C$ go HIGH. The two latches can be strobed individually by using the $\overline{E}_n$ inputs, or simultaneously by using the $\overline{E}_C$ input.

The Set and Reset inputs are effective only if $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH. Note that in this mode of operation the output voltage levels of a latch are unpredictable if both the S and R signals are HIGH.

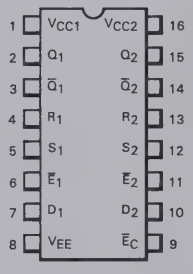
LOGIC SYMBOL



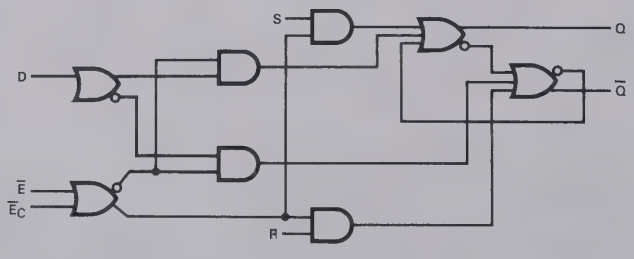
LEAD NAMES

$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
S_n	Set
R_n	Reset
D_n	Data Inputs
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



(1/2 OF CIRCUIT SHOWN)

TRUTH TABLE

D	$\overline{E}_n$	$\overline{E}_C$	S	R	Q_{n+1}	OPERATION
L	L	L	X	X	L	D Function
H	L	L	X	X	H	D Function
X	H	X	L	L	Q_n	Memory
X	X	H	L	L	Q_n	Memory
X	H	X	H	L	H	Set
X	X	H	H	L	H	Set
X	H	X	L	H	L	Reset
X	X	H	L	H	L	Reset
X	H	X	H	H	-	Electrically Indeterminate
X	X	H	H	H	-	Electrically Indeterminate

L = LOW Voltage Level X = Don't Care

H = HIGH Voltage Level Q_n = Output

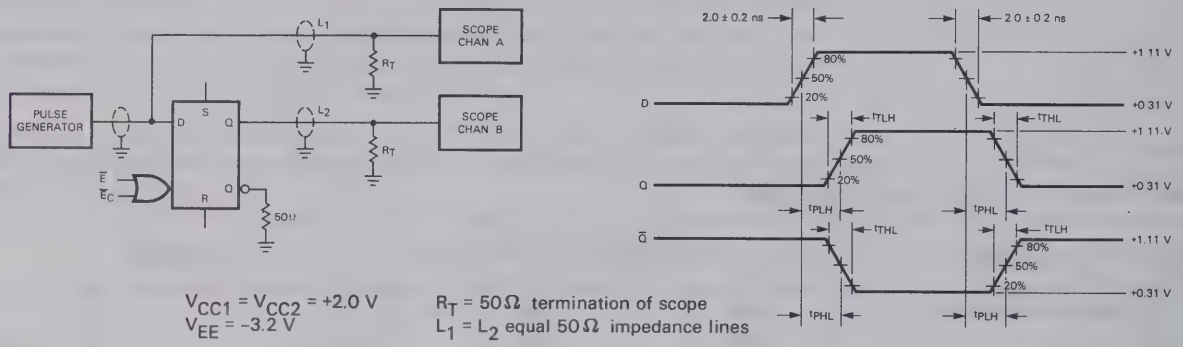
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to –2.0 V
		–960		–810		25°C		
		–900		–720		75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		25°C		
		–1830		–1625		75°C		
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
		–980				25°C		
		–920				75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		25°C		
				–1605		75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		25°C		
		–1045		–720		75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		25°C		
		–1830		–1450		75°C		
I_{IH}	Input Current HIGH				µA	25°C	$V_{IN} = V_{IHA}$	
	$\overline{E}_n$			220				
	$\overline{E}_C$			265				
	D_n			285				
	S_n and R_n			285				
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–35	–25		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	See Figure 1
t_{PLH}	Propagation Delay Set to Output	1.0	2.7	3.5	ns	See Figure 2
t_{PHL}	Propagation Delay Clear to Output	1.0	2.7	3.5	ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20%–80%)	1.5	2.5	3.5	ns	See Figures 1, 2, and 3
t_{THL}	Output Transition Time HIGH to LOW (80%–20%)	1.5	2.5	3.5	ns	
t_s	Set-Up Time Data to Enable	2.5			ns	
t_h	Hold Time Data to Enable	1.5			ns	

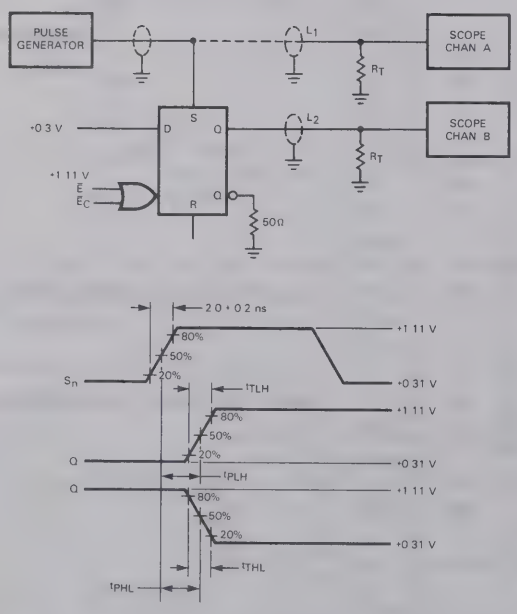
SWITCHING CIRCUITS AND WAVEFORMS



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

$R_T = 50\Omega$ termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

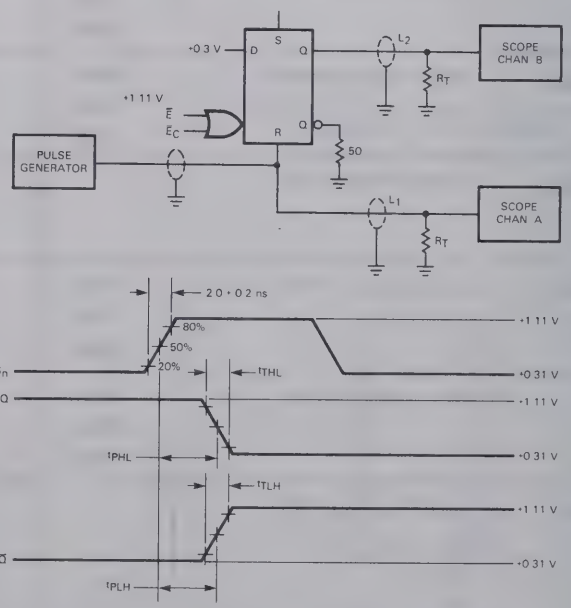
Fig. 1



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

$R_T = 50\Omega$ termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 2



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

$R_T = 50\Omega$ termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 3

F10131

HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION — The F10131 contains two master/slave D-type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

LEAD NAMES

D_n	Data Input to Master
CP_n	Clock Input
CP_C	Common Clock Input
Q_n	Output
$\overline{Q}_n$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

TRUTH TABLES

SYNCHRONOUS OPERATION
D TABLE

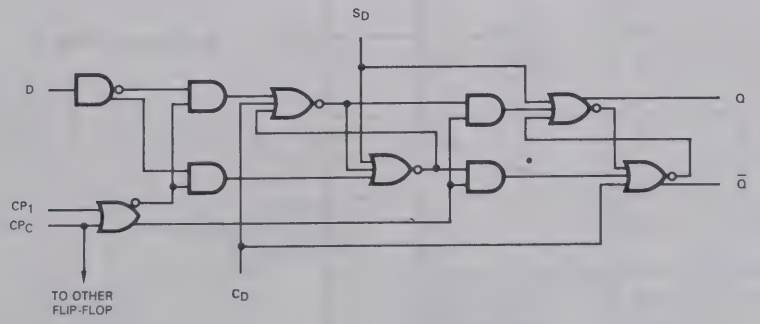
D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

(t+1) = Time after positive going clock transition

ASYNCHRONOUS OPERATION
S_D C_D TABLE

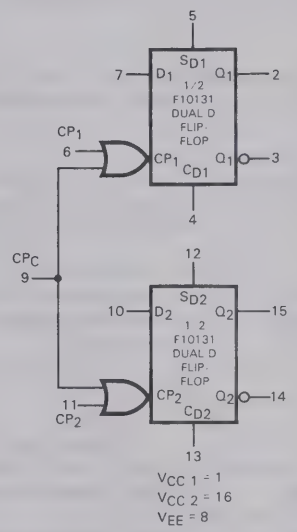
C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC DIAGRAM

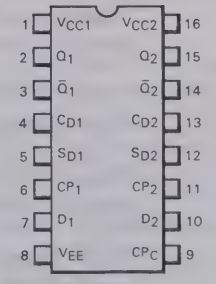


Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



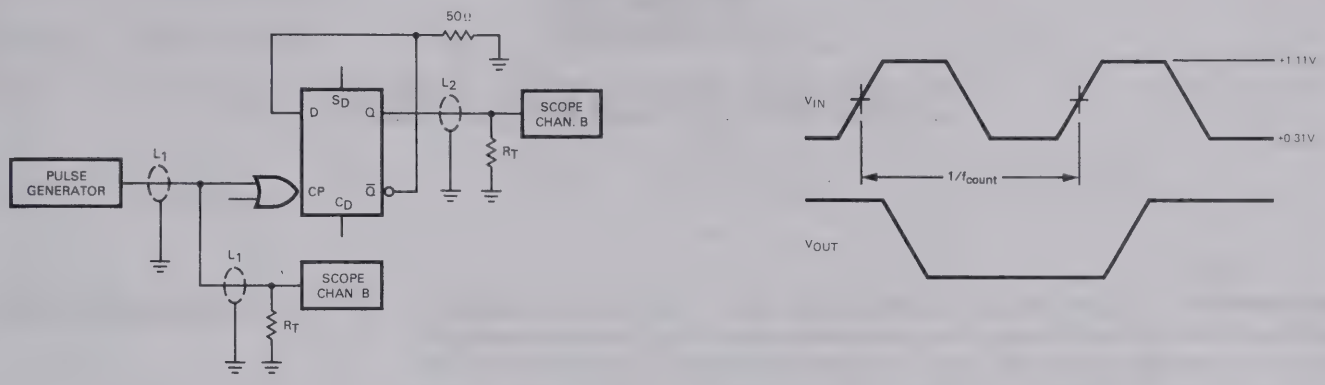
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS		
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH CP C_{CP} D S_D & C_D			 220 265 245 330	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–56	–45		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

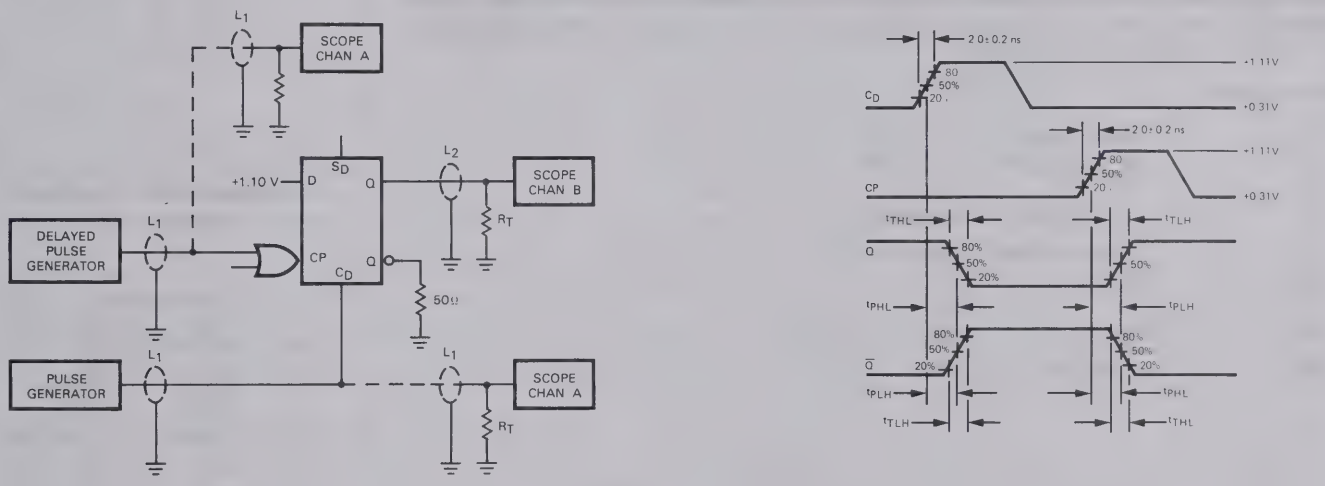
f_{count}	Toggle Frequency	125	160		MHz		See Figure 1
t_{PLH}	Propagation Delay Clock to Output	1.5	3.0	4.5	ns		See Figure 2 and 3
t_{PHL}	Propagation Delay Clock to Output	1.5	3.0	4.5	ns		
t_{PLH}	Propagation Dealy Set to Q, Clear to $\overline{Q}$	1.2	2.2	4.3	ns		
t_{PHL}	Propagation Delay Set to $\overline{Q}$, Clear to Q	1.2	2.2	4.3	ns		
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	4.5	ns		
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	4.5	ns		
t_s	Set-Up Time Data to Clock	2.5	0.5		ns		
t_h	Hold Time Data to Clock	1.5	–0.5		ns		

SWITCHING CIRCUITS AND WAVEFORMS



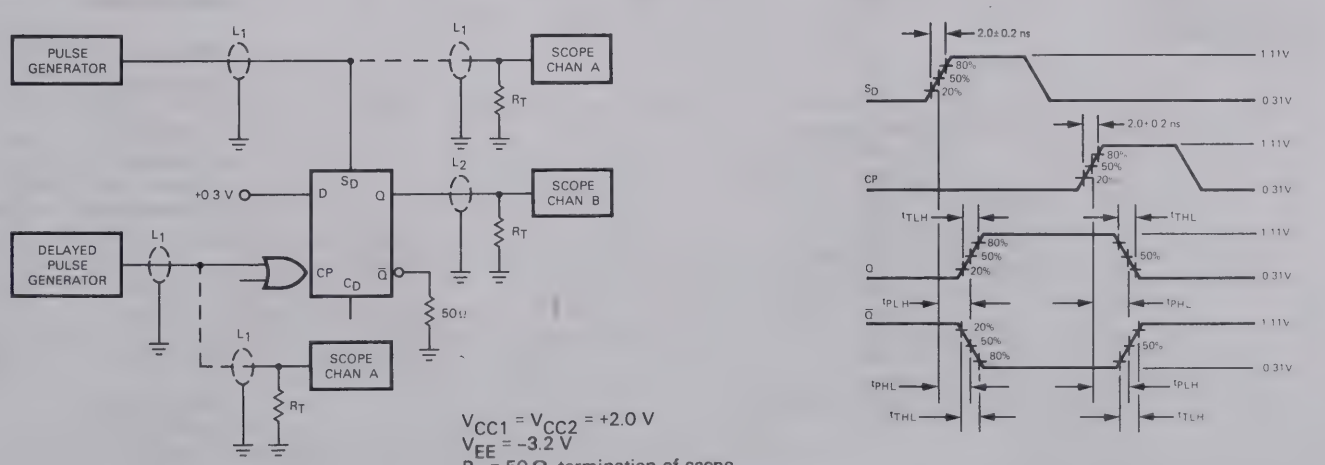
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\,\Omega$ termination of scope
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}

Fig. 1. Toggle Rate Test Circuit



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\,\Omega$ termination of scope
$L_1 = L_2$ equal $50\,\Omega$ impedance lines
All input transition times are 2 + 0.2 ns

Fig. 2. Propagation Delay and C_D Test Circuit



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\,\Omega$ termination of scope
$L_1 = L_2$ equal $50\,\Omega$ impedance lines
All input transition times are 2 + 0.2 ns

Fig. 3. Propagation Delay & S_D Test Circuit

F10132

DUAL MULTIPLEXER/LATCH

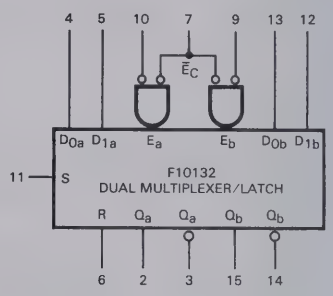
DESCRIPTION — The F10132 is a dual multiplexer with D type latches and has common Data Select and Reset inputs. Each latch may be enabled separately by holding the Common Enable ($\overline{E}_C$) in the LOW state or by using the Enable ($\overline{E}_n$) inputs. If the Common Enable is used to enable the latch, the $\overline{E}_n$ inputs must be in the LOW state. In this mode, the $\overline{E}_n$ inputs perform the function of controlling $\overline{E}_C$.

The Data Select (S) input determines which Data input is enabled. A HIGH input enables Data inputs D_{1a} and D_{1b} and a LOW input enables Data inputs D_{0a} and D_{0b}. Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information. The Reset input is enabled when $\overline{E}_C$ or both $\overline{E}_a$ and $\overline{E}_b$ are in the HIGH state.

LEAD NAMES

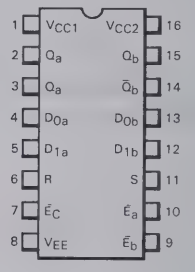
S	Data Select
D_n	Data Input
$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
R	Reset
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

LOGIC SYMBOL

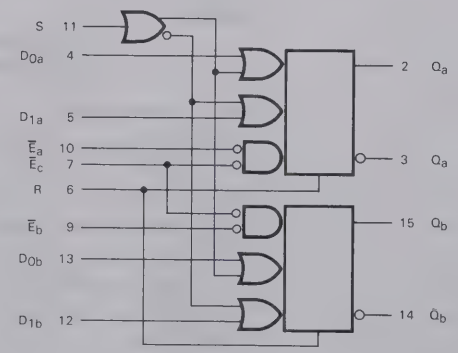


V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE

R	D	$\overline{E}_C$	$\overline{E}_n$	Q_{n+1}
L	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	X	X	H	L

L = LOW Logic Level
H = HIGH Logic Level
X = Don't Care

$D = (\overline{S} \bullet D_{0a}) + (S \bullet D_{1a})$

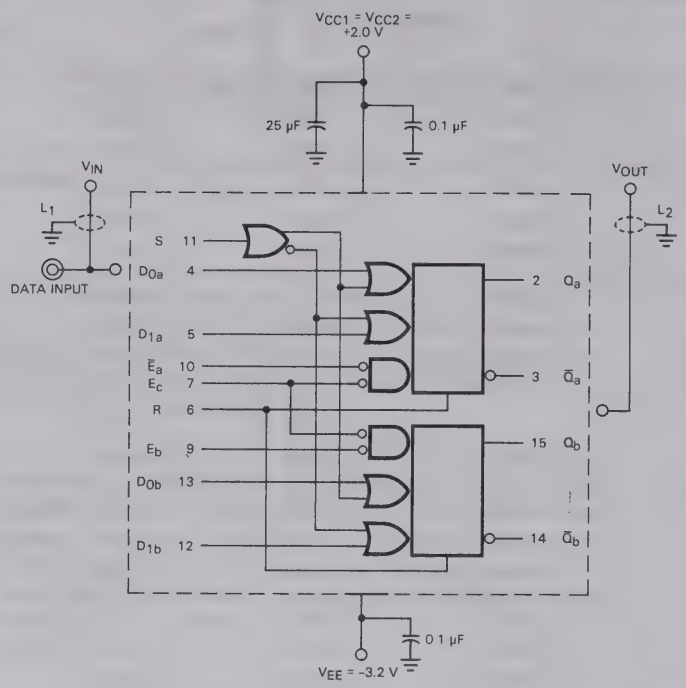
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Select and Enable Data and Common Enable Reset			 265 290 390	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-55			mA	25°C	Inputs and Outputs Open	

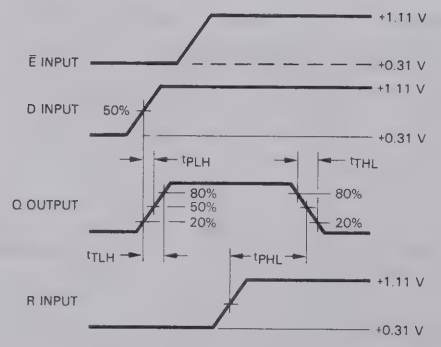
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

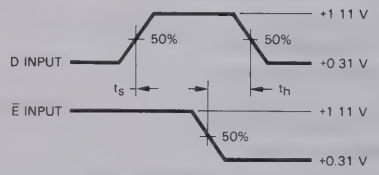
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output		4.5		ns	See Figure 1
t_{PHL}	Propagation Delay Select to Output		3.7		ns	
t_{PLH}	Propagation Delay Data to Output		3.5		ns	
t_{PHL}	Propagation Delay Reset to Output		2.5		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
t_s	Set-Up Time Data Select		 1.5 2.5		 ns	
t_h	Hold Time Data Select		 0.0 -0.5		 ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V





NOTE:

t_s is the minimum time before the transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the transition of the enable pulse that information must remain unchanged at the data input (D).

Fig. 1

F10133

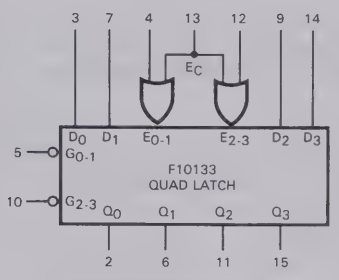
QUAD LATCH

DESCRIPTION — The F10133 is a high speed low power Quad Latch consisting of four bistable latch circuits with D type inputs and gated outputs.

Open emitters allow a large number of outputs to be wired-OR together and latch outputs are gated, allowing direct wiring to a bus.

When either Enable is HIGH, outputs will follow the Data inputs. Information is latched on the negative going transition of the enable.

LOGIC SYMBOL

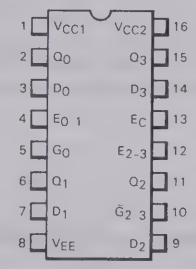


V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

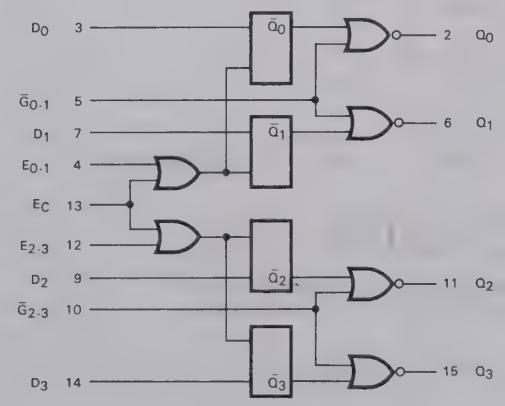
LEAD NAMES

D_n	Data Input
$\overline{G}_n$	Gate Input (Active LOW)
E_n	Enable (Active HIGH)
E_C	Common Enable (Active HIGH)
Q_n	Output

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE

$\overline{G}$	E	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

L = LOW Logic Level
H = HIGH Logic Level
X = Don't Care

$E = E_C + E_n$

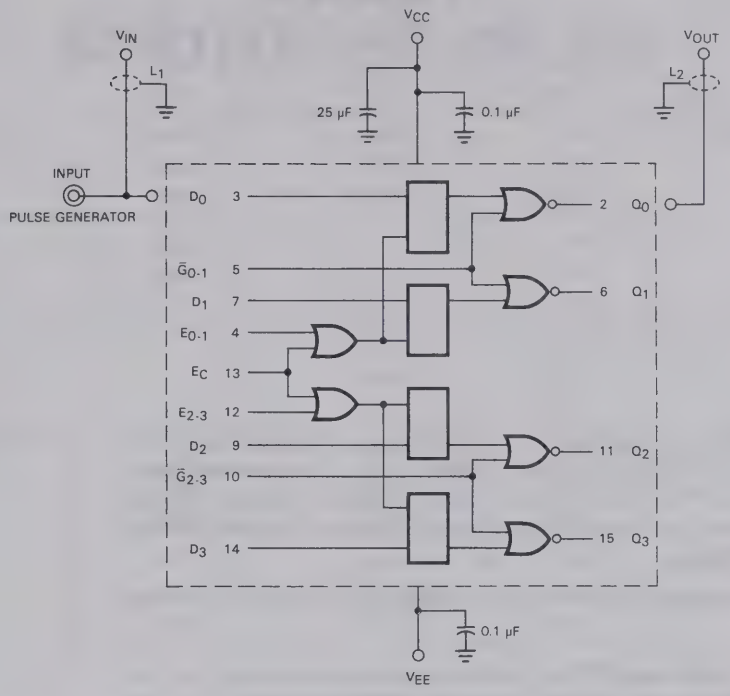
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Data Common Enable Gate and Enable			 245 265 350	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	75			mA	25°C	Inputs and Outputs Open	

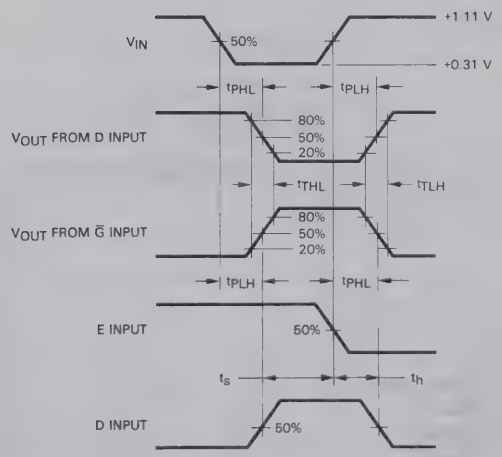
SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output	1.0	4.0	5.4	ns	See Figure 1
t_{PHL}	Propagation Delay Data to Output	1.0	4.0	5.4	ns	
t_{PLH}	Propagation Delay Gate to Output	1.0	2.0	3.1	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.5	ns	
t_s	Set-Up Time Data		0.7	2.5	ns	
t_h	Hold Time Data		0.7	1.5	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



t_s is minimum time before the negative transistion of the enable pulse (E) that information must be present at the data input (D).

t_h is the minimum time after the negative transition of the enable pulse (E) that information must remain unchanged at the data input (D).

Fig. 1

F10134
DUAL MULTIPLEXER/LATCH

DESCRIPTION — The F10134 is a Dual Multiplexer with D type latches. Each latch may be enabled separately by holding the Common Enable in the LOW state and using the Enable ($\overline{E}_n$) inputs. If the Common Enable ($\overline{E}_C$) is used to enable the latch, the $\overline{E}_n$ inputs must be in the LOW state. In this mode, the Enable inputs perform the function of controlling the Common Enable.

The Data Select inputs determine which Data input is enabled, as indicated in the Truth Table and Logic Diagram.

Any change on the Data input is reflected at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the Enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

LEAD NAMES

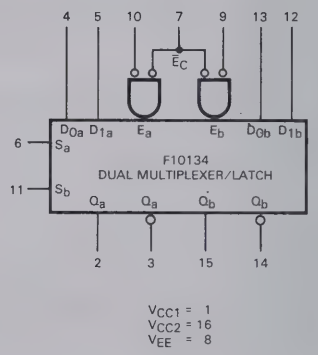
S_n	Data Select
D_n	Data Inputs
$\overline{E}_n$	Enable (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
Q_n	Outputs
$\overline{Q}_n$	Outputs (Active LOW)

TRUTH TABLE

$\overline{E}$	S_a	D_{0a}	D_{1a}	Q_{n+1}
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Q_n

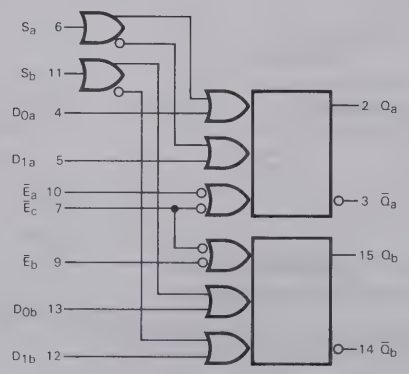
$\overline{E} = \overline{E}_n + \overline{E}_c$
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

LOGIC SYMBOL



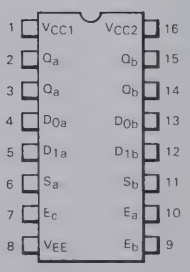
V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

CONNECTION DIAGRAM
DIP (TOP VIEW)



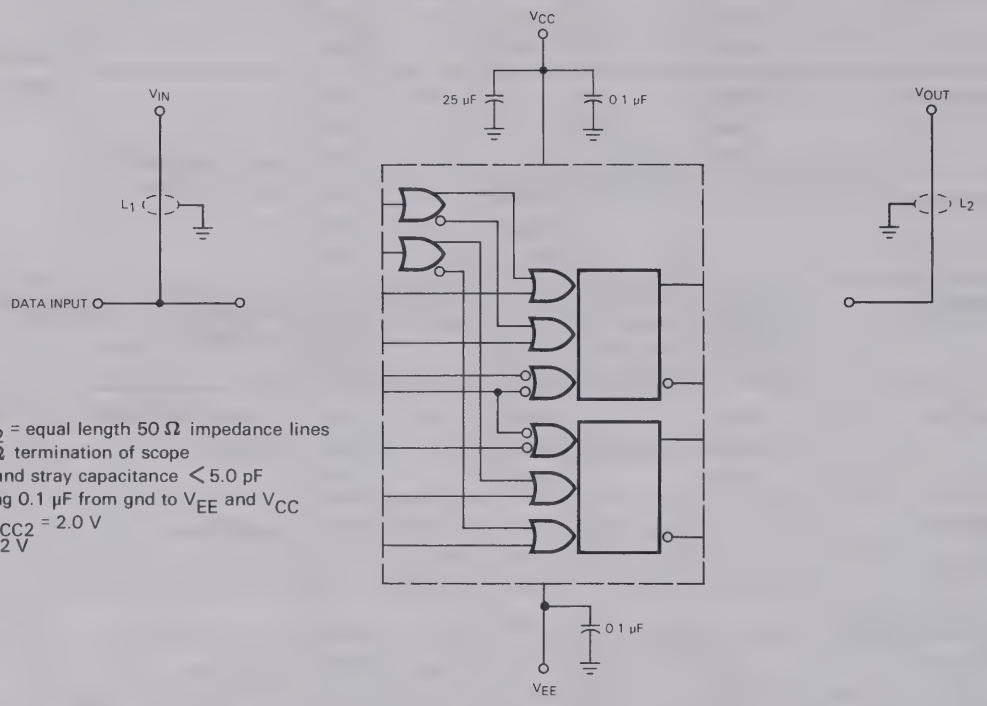
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Enable Select Data and Common Enable			 265 265 290	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–55			mA	25°C	Inputs and Outputs Open	

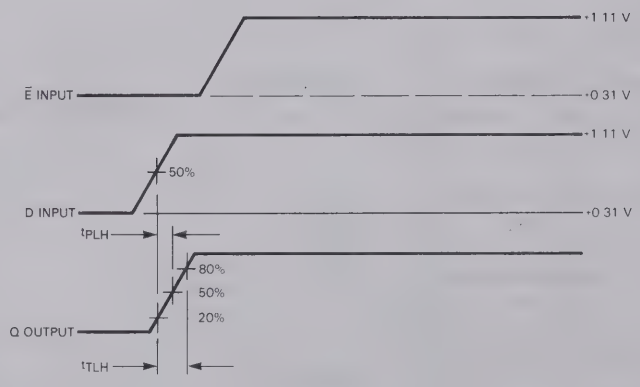
SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

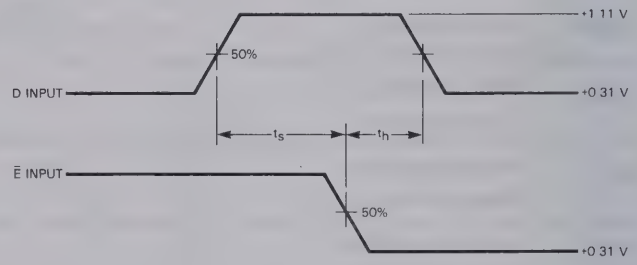
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Clock to Output		4.5		ns	See Figure 1
t_{PHL}	Propagation Delay Data to Output		3.0		ns	
t_{PLH}	Propagation Delay Select to Output		3.7		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
t_s	Set-Up Time Data Select		 1.5 2.5		ns	
t_h	Hold Time Data Select		 0.0 –0.5		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V





NOTE:

t_s is the minimum time before the positive transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

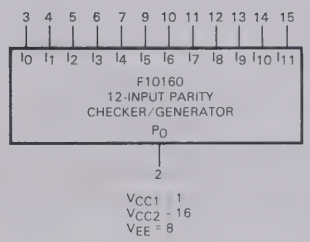
Fig. 1

F10160

12-BIT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10160 is a 12-Input Parity Generator. The output will be HIGH when an odd number of inputs are HIGH; typical delay is 4 ns. For applications requiring fewer than 12 inputs, unused inputs may be left open, since internal input resistors hold unconnected inputs LOW.

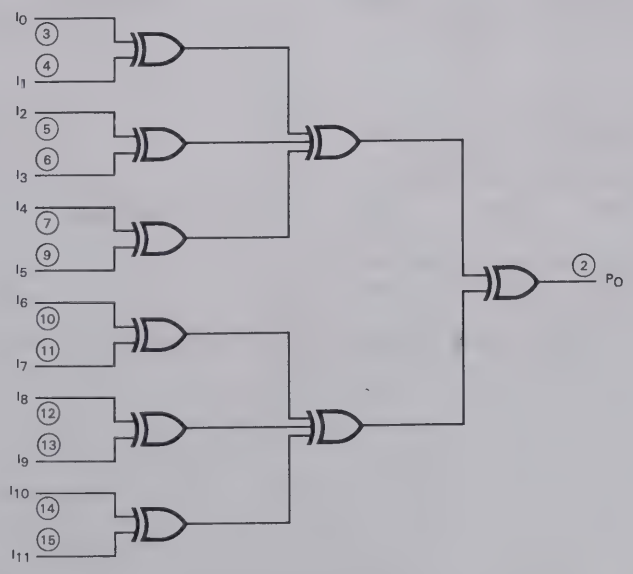
LOGIC SYMBOL



LEAD NAMES

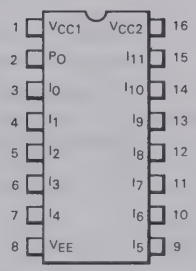
I_n	Inputs
P_O	Parity Odd

LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



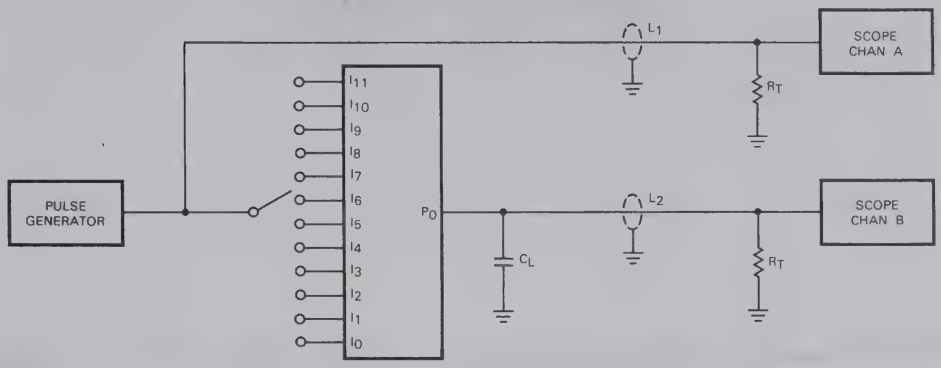
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Logic Function	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH (All Inputs)			220	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–59	–46		mA	25°C	Inputs and Outputs Open	

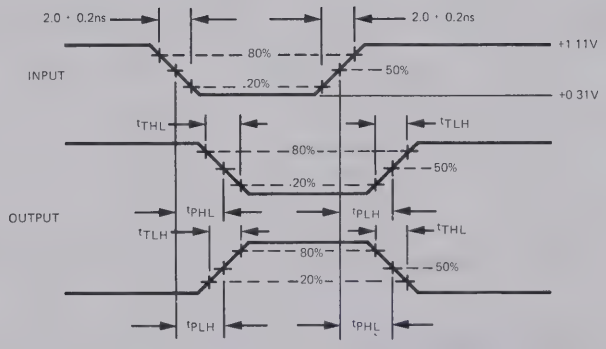
SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH		4.0		ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW		4.0		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



$L_1 = L_2$ = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF



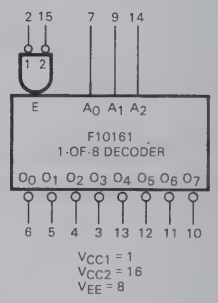
Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = −3.2 V

Fig. 1

F10161
1-OF-8 DECODER
ACTIVE LOW OUTPUTS

DESCRIPTION — The F10161 accepts a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be LOW while all other outputs are HIGH. Two enable inputs force all outputs HIGH when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

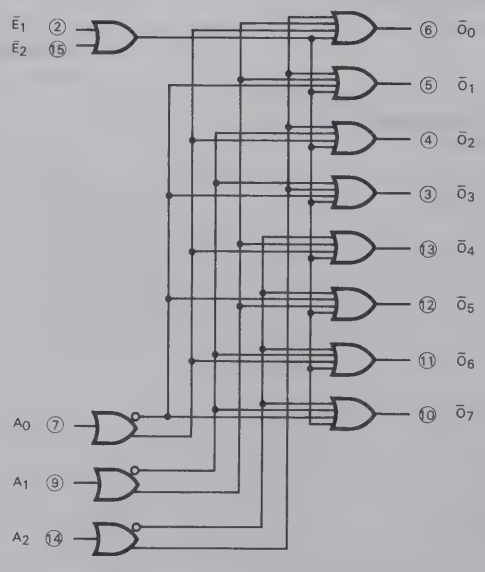
LOGIC SYMBOL



LEAD NAMES

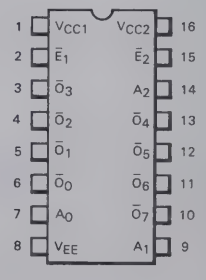
$\overline{E}_n$	Enable (Active LOW)
A_n	Address Inputs
$\overline{O}_n$	Output (Active LOW)

LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\bar{E}_2$	$\bar{E}_1$	A_2	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

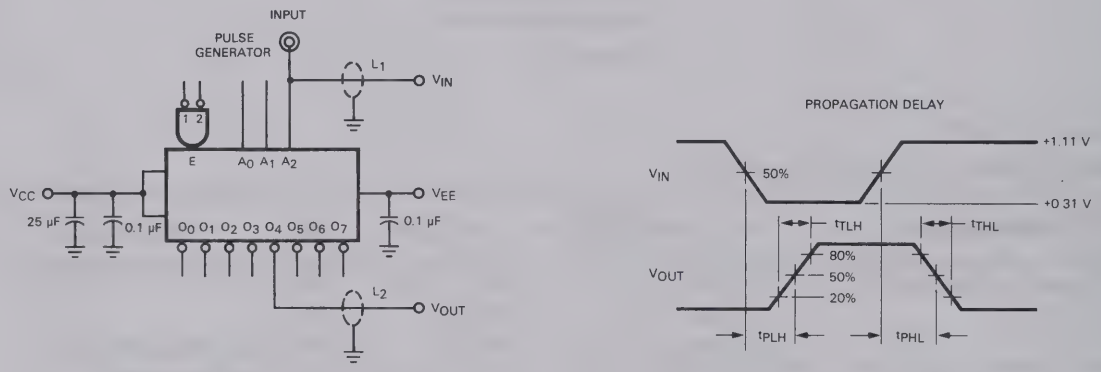
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-76	-55		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 1.

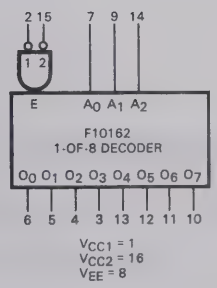
F10162
1-OF-8 DECODER
ACTIVE HIGH OUTPUTS

DESCRIPTION — The F10162 accepts a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be HIGH while all other outputs are LOW. Two enable inputs force all outputs LOW when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

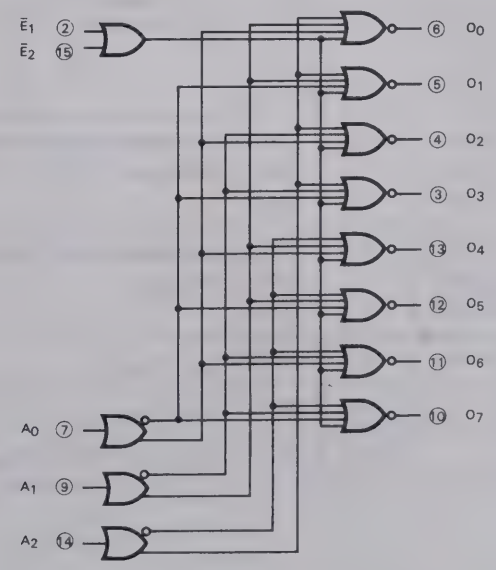
LEAD NAMES

$\overline{E}_n$	Enable (Active LOW)
A_n	Address Inputs
O_n	Output (Active HIGH)

LOGIC SYMBOL

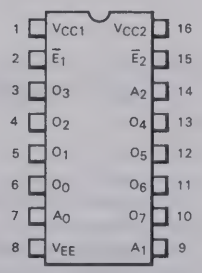


LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

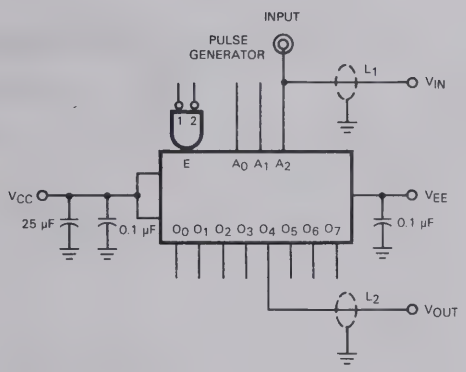
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

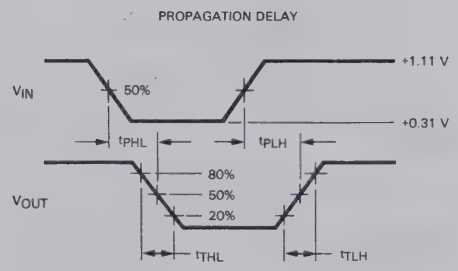
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–76	–55		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 1.

F10164

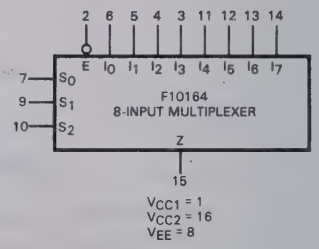
8-INPUT MULTIPLEXER

DESCRIPTION — The F10164 accepts a 3-bit address and selects 1-of-8 inputs. The enable line, when HIGH, forces the output LOW. Typical address to output delays are 4 ns.

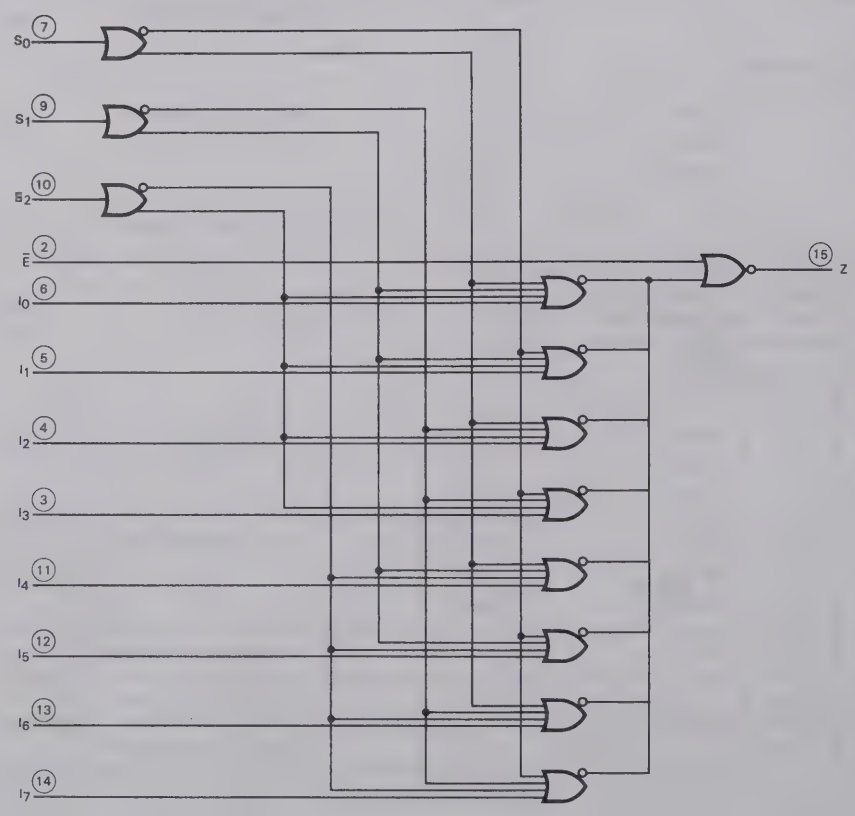
LEAD NAMES

$\overline{E}$	Enable (Active LOW)
I_n	Inputs
S_n	Select Inputs
Z	Output

LOGIC SYMBOL

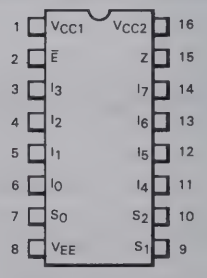


LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\overline{\text{ENABLE}}$	ADDRESS INPUTS			Z
	S_2	S_1	S_0	
L	L	L	L	I_0
L	L	L	H	I_1
L	L	H	L	I_2
L	L	H	H	I_3
L	H	L	L	I_4
L	H	L	H	I_5
L	H	H	L	I_6
L	H	H	H	I_7
H	X	X	X	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

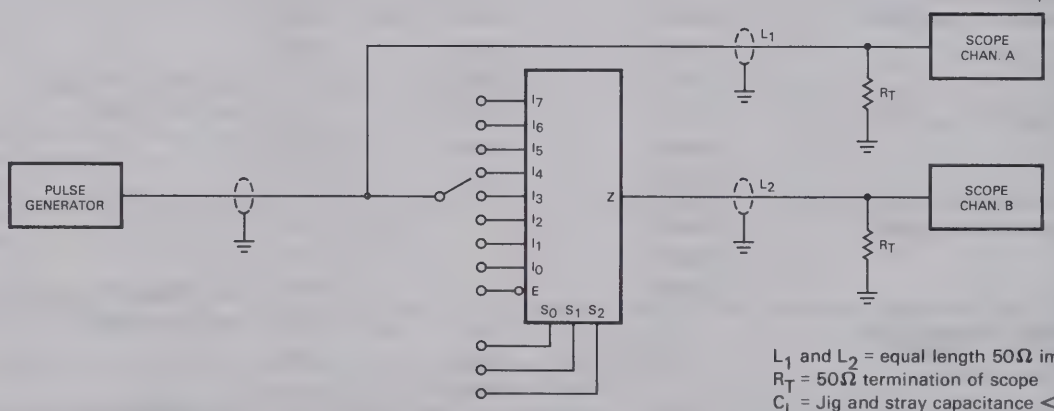
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$, All Other Leads Open	
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-75	-55		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay Input to Output	1.5	3.0	4.5	ns	Figure 1
t_{PHL}	Propagation Delay Input to Output	1.5	3.0	4.5	ns	
t_{PLH}	Propagation Delay Address to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Address to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{PLH}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{THL}	Output Transition Time HIGH to LOW	1.5	2.0	3.3	ns	
t_{TLH}	Output Transition Time LOW to HIGH	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

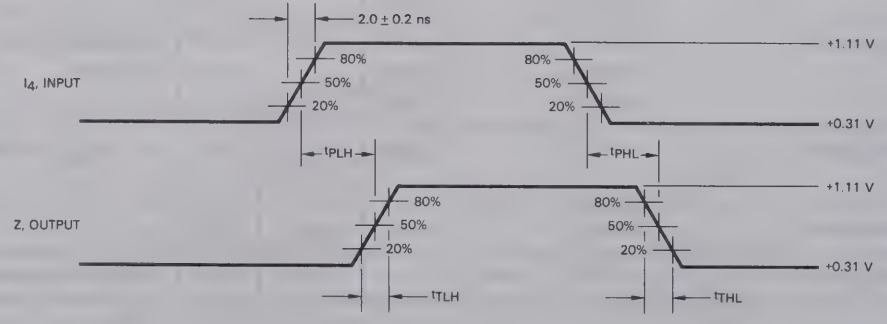


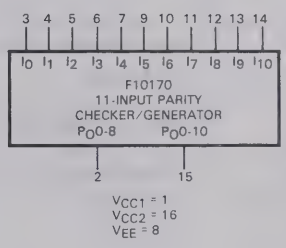
Fig. 1

F10170

11-INPUT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10170 is a very high speed 11-Input Parity Checker/Generator. It is useful for data processing, memory and data transmission applications. Two outputs are provided; $P_O0\text{-}8$ is HIGH when there is an odd number of HIGH inputs on I_0, I_1 to I_8. The output $P_O0\text{-}10$ will be HIGH if there is an odd number of HIGH inputs on I_0, I_1 to I_{10}. Unused inputs are held LOW by internal load resistors. Note from the logic diagram that there is only a single gate delay from inputs I_9 and I_{10} to the output $P_O0\text{-}10$ making them ideal for expansion when more than 11 inputs are required. Typical propagation delays are 4 ns from inputs I_0 - I_8 to output $P_O0\text{-}8$, and 6 ns to output $P_O0\text{-}10$. Typical delay from I_9 and I_{10} to $P_O0\text{-}10$ is 2 ns.

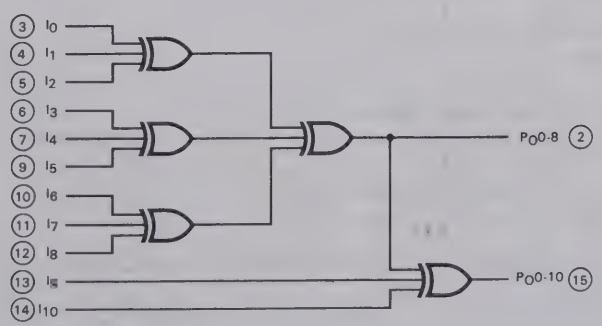
LOGIC SYMBOL



LEAD NAMES

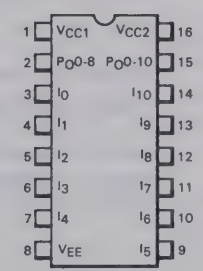
I_n	Inputs
P_O	Parity Odd

LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



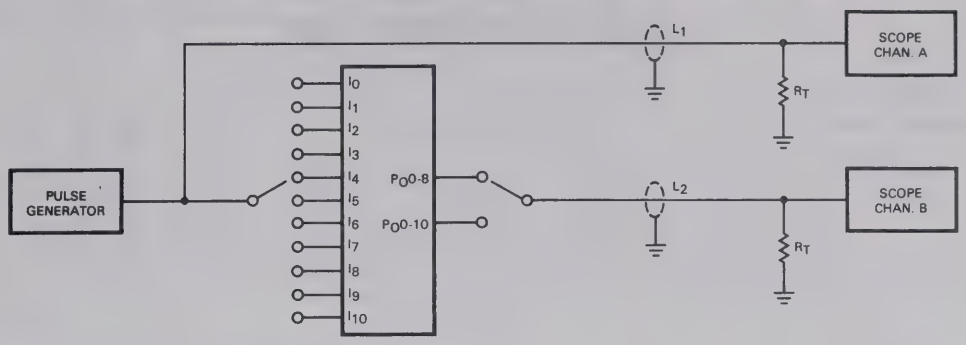
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Logic Function	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH (All Inputs)			220	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–68	–53		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH		4.0		ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW		4.0		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORM



Unused outputs connected to a 50 Ω resistor to ground.

L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

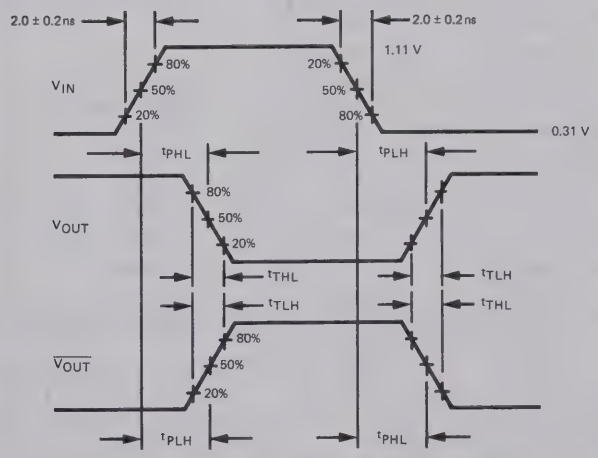


Fig. 1.

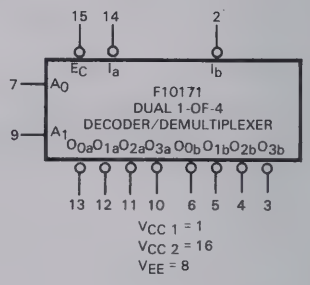
F10171
DUAL 1-OF-4 DECODER/DEMULTIPLEXER
SELECTED OUTPUTS LOW

DESCRIPTION — The F10171 contains a pair of 1-of-4 Decoder/Multiplexers with Common Enable ($\overline{E}_C$) and Address (A_0 and A_1) inputs. In each decoder the unselected (or disabled) outputs are HIGH and the selected (or enabled) output repeats the information present on its data input ($\overline{I}_a$ or $\overline{I}_b$). If the $\overline{E}_C$ input is HIGH all outputs of both decoders are HIGH, as indicated in the truth table. The F10171 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to $\overline{I}_a$ and $\overline{I}_b$, respectively, and using $\overline{E}_C$ as either a data input or as an enable.

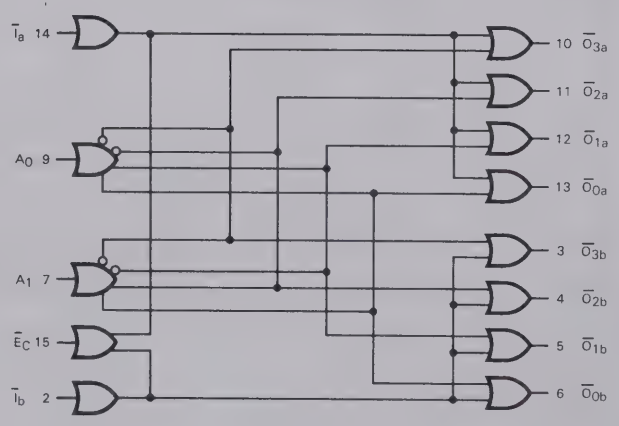
LEAD NAMES

$\overline{E}_C$	Common Enable (Active LOW)
A_n	Address Inputs
$\overline{I}_n$	Data Inputs
$\overline{O}_n$	Outputs

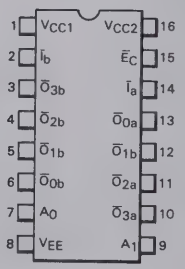
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\overline{E}_C$	$\overline{I}_a$ $\overline{I}_b$	A_1	A_0	$\overline{O}_{0a}$ $\overline{O}_{0b}$	$\overline{O}_{1a}$ $\overline{O}_{1b}$	$\overline{O}_{2a}$ $\overline{O}_{2b}$	$\overline{O}_{3a}$ $\overline{O}_{3b}$
L	L	L	L	L	H	H	H
L	H	L	L	H	H	H	H
L	L	L	H	H	L	H	H
L	H	L	H	H	H	H	H
L	L	H	L	H	H	L	H
L	H	H	L	H	H	H	H
L	L	H	H	H	H	H	L
L	H	H	H	H	H	H	H
H	X	X	X	H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

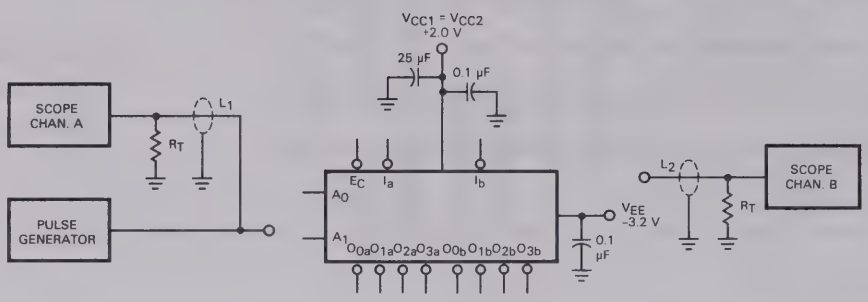
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75 'C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-77	-62		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.1	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.1	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

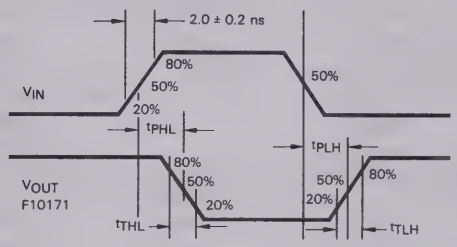


Fig. 1

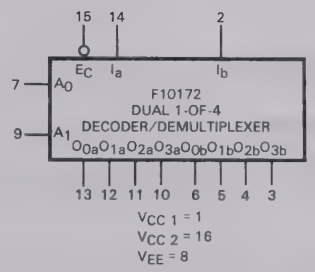
F10172
DUAL 1-OF-4 DECODER/DEMULTIPLEXER
SELECTED OUTPUTS HIGH

DESCRIPTION — The F10172 contains a pair of 1-of-4 Decoder/Multiplexers with Common Enable ($\bar{E}_C$) and Address (A_0 and A_1) inputs. In each decoder the unselected (or disabled) outputs are LOW and the selected (or enabled) output repeats the information present on its data input (I_a or I_b). If the $\bar{E}_C$ input is HIGH all outputs of both decoders are LOW, as indicated in the truth table. The F10172 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to I_a and I_b, respectively, and using $\bar{E}_C$ as either a data input or as an enable.

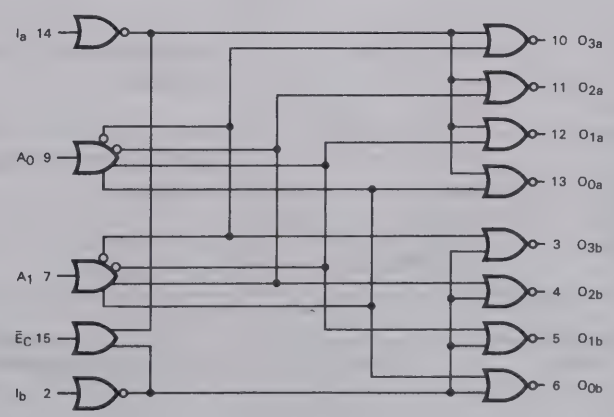
LEAD NAMES

$\bar{E}_C$	Common Enable (Active LOW)
A_n	Address Inputs
I_n	Data Inputs
O_n	Outputs

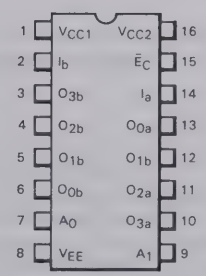
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\bar{E}_C$	I_a I_b	A_1	A_0	O_{0a} O_{0b}	O_{1a} O_{1b}	O_{2a} O_{2b}	O_{3a} O_{3b}
L	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L
L	L	L	H	L	L	L	L
L	H	L	H	L	H	L	L
L	L	H	L	L	L	L	L
L	H	H	L	L	L	H	L
L	L	H	H	L	L	L	L
L	H	H	H	L	L	L	H
H	X	X	X	L	L	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

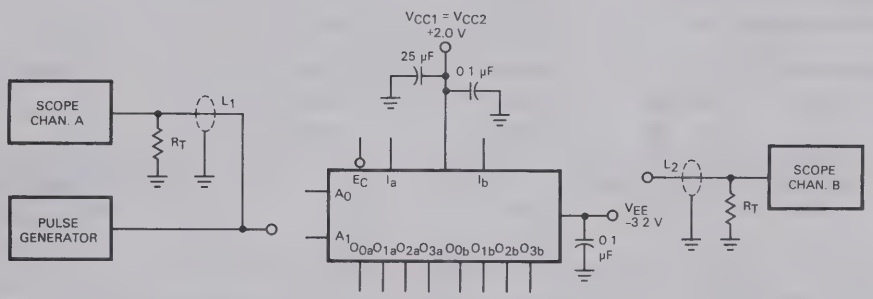
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS		
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-77	-62		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.1	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.1	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

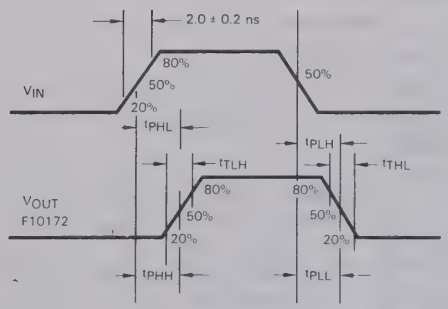


Fig. 1

F10173

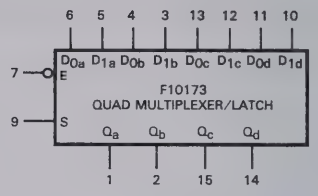
QUAD MULTIPLEXER/LATCH

DESCRIPTION — The F10173 is a Quad 2-Channel Multiplexer with latches. It incorporates a common Enable and a common Data Select input. The Select input determines which Data input is enabled. A HIGH input enables Data inputs D_{0a}, D_{0b} D_{0c}, and D_{0d} and a LOW enables Data inputs D_{1a}, D_{1b}, D_{1c}, D_{1d}. Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable input is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

LEAD NAMES

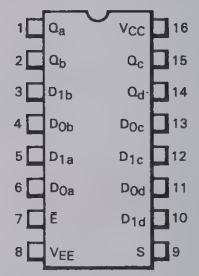
S	Data Select
D_n	Data Inputs
$\overline{E}$	Enable (Active LOW)
Q_n	Outputs

LOGIC SYMBOL

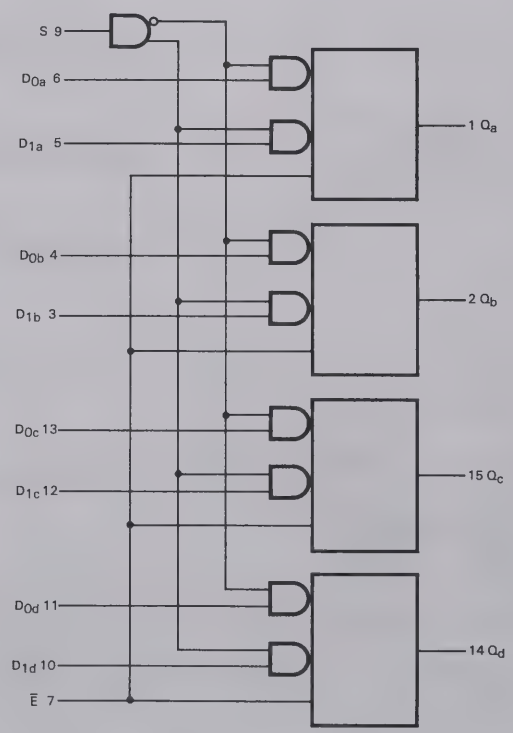


V_{CC} = 16
V_{EE} = 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE

S	$\overline{E}$	Q_{n+1}
H	L	D_{0a}
L	L	D_{1a}
X	H	Q_n

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

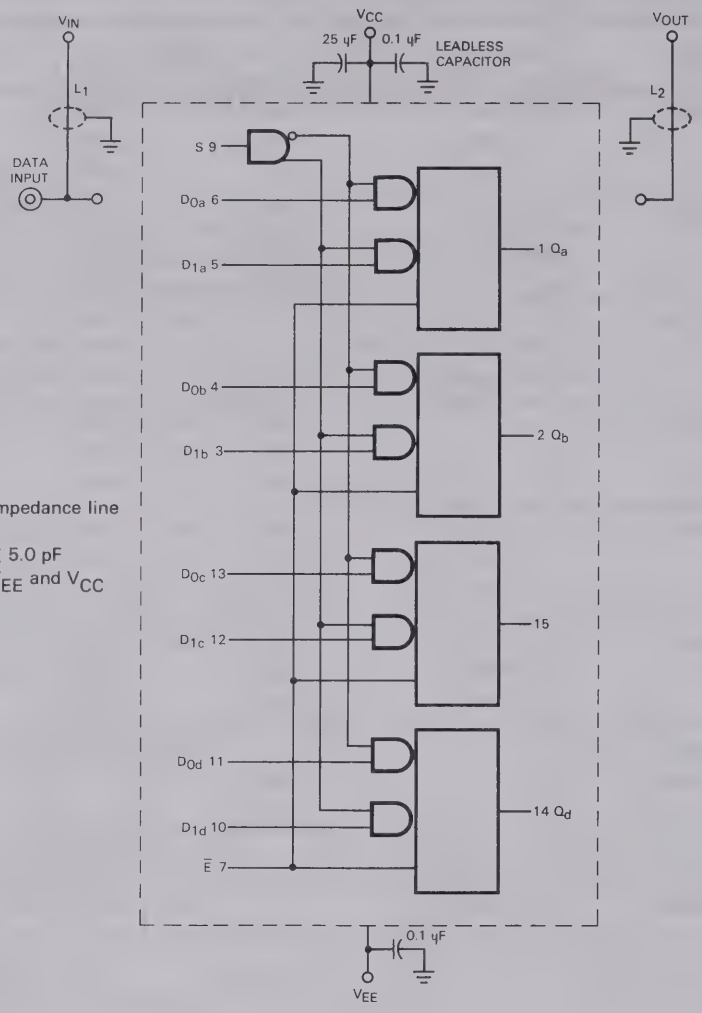
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Enable and Select Data			 245 290	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-66			mA	25°C	Inputs and Outputs Open	

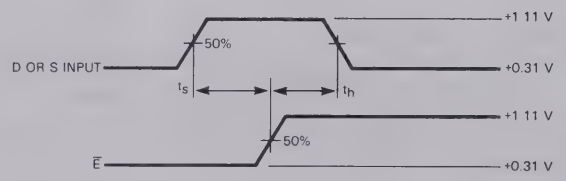
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output		4.5		ns	See Figure 1
t_{PHL}	Propagation Delay Data to Output		2.5		ns	
t_{PLH}	Propagation Delay Select to Output		3.5		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
t_s	Set-Up Time Data Select		 1.5 2.5		ns	
t_h	Hold Time Data Select		 0.0 -0.5		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance line
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
V_{CC} = 2.0 V
V_{EE} = -3.2 V



NOTE:

t_s is the minimum time before the positive transition of the enable pulse (E) that information must be present at the input (D) or (S).

t_h is the minimum time after the positive transition of the enable pulse (E) that information must remain unchanged at the data input (D) or (S).

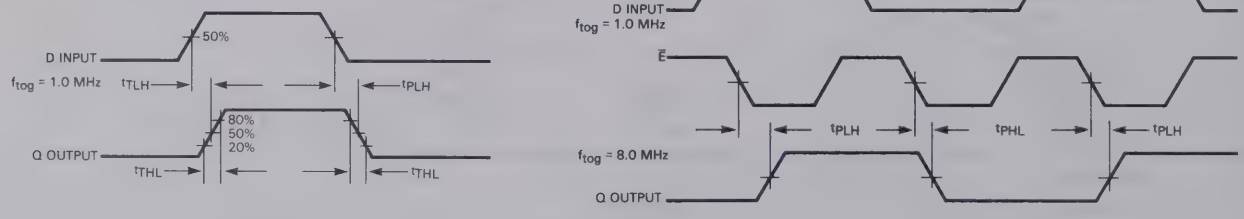


Fig. 1

F10174

DUAL MULTIPLEXER

DESCRIPTION — The F10174 is a high speed Dual Channel Multiplexer with output enable capability. The Select inputs determine one of four active Data inputs for each multiplexer. When the Enable input is HIGH, both outputs are forced LOW. The Enable is also useful when OR-wiring several multiplexers to achieve additional channel capability.

LEAD NAMES

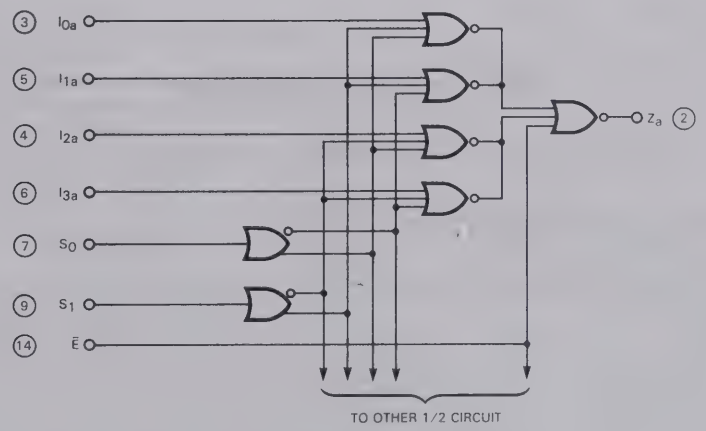
I_n	Address Inputs
$\overline{E}$	Enable (Active LOW)
Z_a	Outputs
S_n	Select Inputs

TRUTH TABLE

$\overline{E}$	S_1	S_0	Z_a	Z_b
H	X	X	L	L
L	L	L	I_{0a}	I_{0b}
L	L	H	I_{1a}	I_{1b}
L	H	L	I_{2a}	I_{2b}
L	H	H	I_{3a}	I_{3b}

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

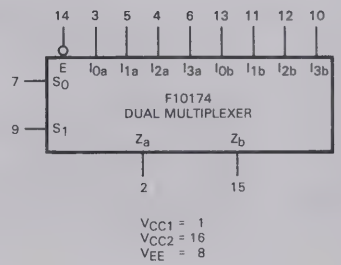
LOGIC DIAGRAM



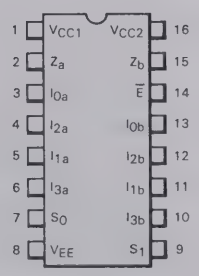
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

○ = LEAD NUMBERS

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



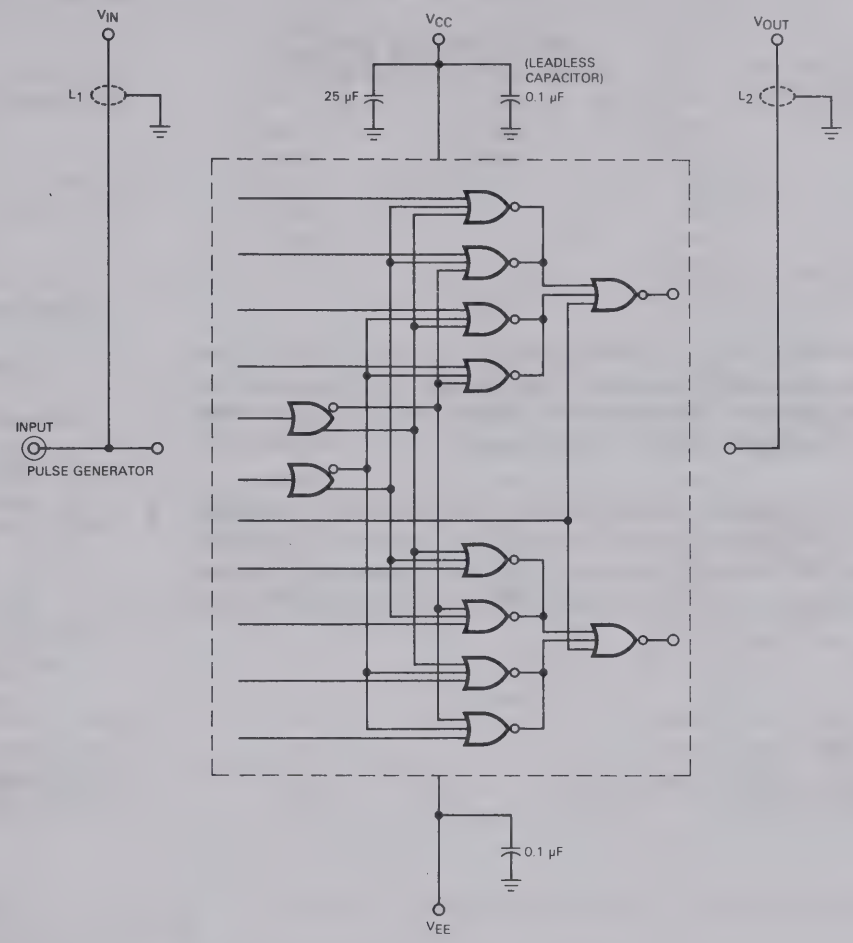
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Data Enable			 220 330	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–50	–40		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}	Propagation Delay Data to Output	1.5	3.0	4.5	ns	See Figure 1
t_{PLH}	Propagation Delay Select to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 uF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

1) Data to Output Delay
   Pulse (V_{IN}) applied to selected data input per truth table.
2) Select to Output Delay
   Pulse (V_{IN}) applied to select input with one selected data input HIGH and the other selected data input LOW per address truth table.
3) Enable to Output Delay
   Selected data input at V_{IH} while the input pulse (V_{IN}) is applied to the enable input.

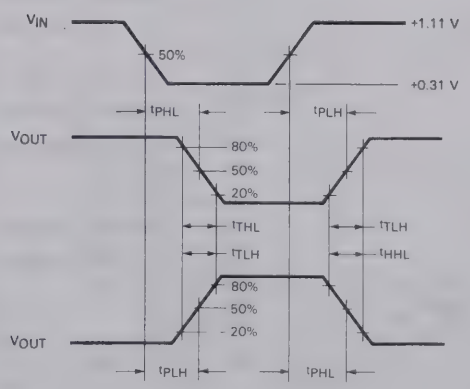


Fig. 1

F10175

QUINT LATCH

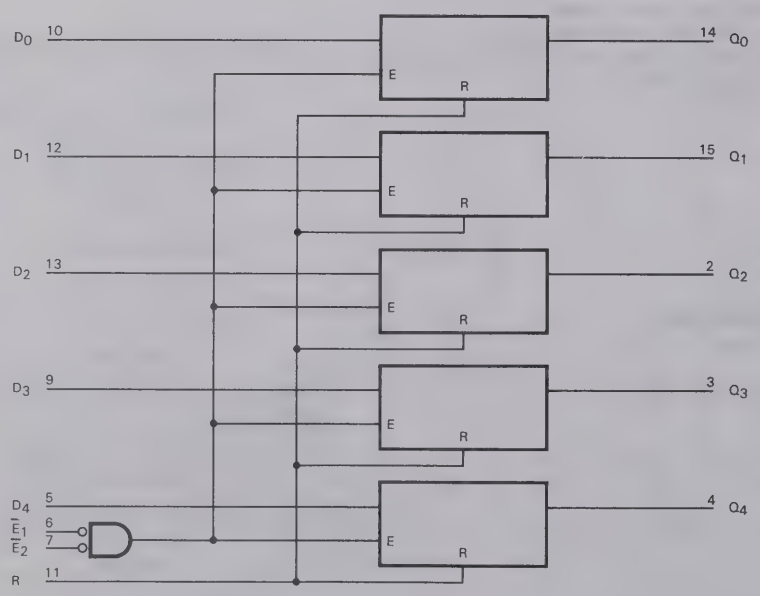
DESCRIPTION — The F10175 is a high speed low power Quint Latch. It features five D type latches with common Reset and a common 2-input Enable. Data is transferred on the negative edge of the enable and latched on the positive edge. The two Enable inputs are OR-ed together. Propagation delays are typically 2.5 ns from each Data input to the output.

Any change on the Data input appears at the outputs while the Enable inputs are LOW. The outputs are latched on the positive transition of the Enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information. The Reset input is enabled only when the Enable is in the HIGH state.

LEAD NAMES

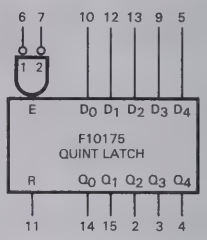
D_n	Data Inputs
$\overline{E}_n$	Enable Inputs (Active LOW)
R	Reset
Q_n	Outputs

LOGIC DIAGRAM



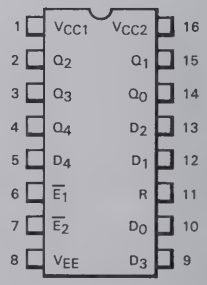
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

CONNECTION DIAGRAM DIP (TOP VIEW)



TRUTH TABLE

D	$\overline{E}_0$	$\overline{E}_1$	R	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q_n
X	X	H	L	Q_n
X	H	X	H	L
X	X	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

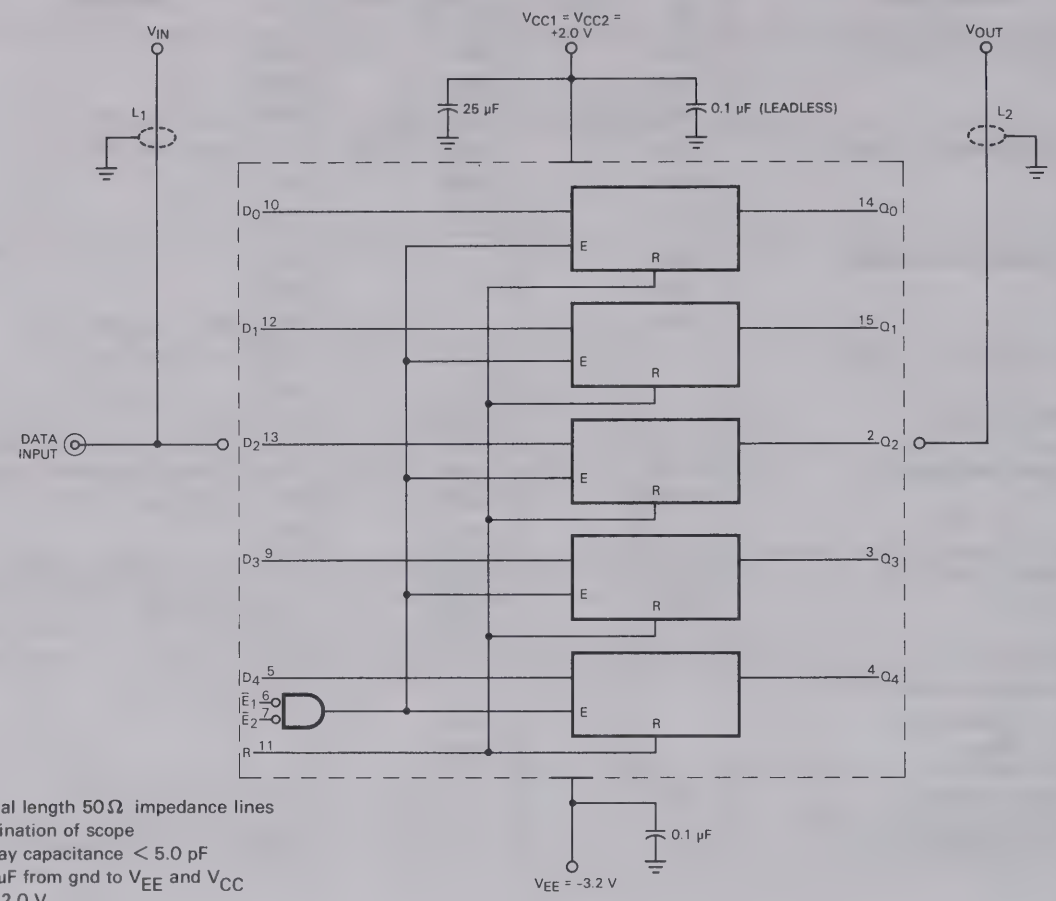
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75 °C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Data Enable Reset			 290 645	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	–97			mA	25°C	Inputs and Outputs Open	

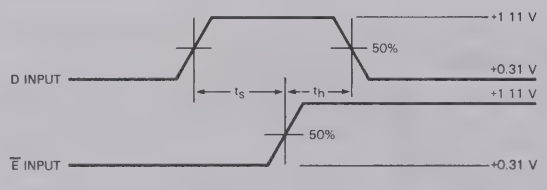
SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output		3.3		ns	See Figure 1
t_{PHL}	Propagation Delay Data to Output		2.5		ns	
t_{PLH}	Propagation Delay Reset to Output		2.5		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
t_s	Set-Up Time Data		1.5		ns	
t_h	Hold Time Data		0.5		ns	

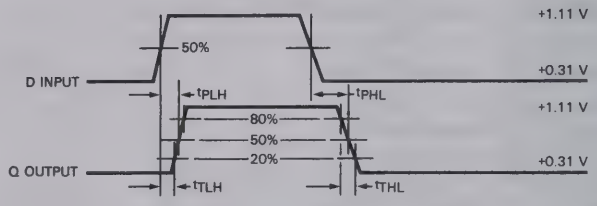
SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



DATA TO OUTPUT (ENABLE LOW)

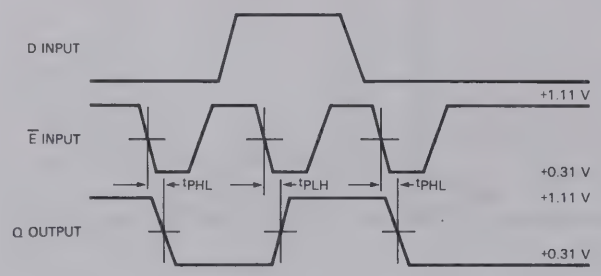


NOTE:

t_s is the minimum time before the positive transition of the enable pulse that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

ENABLE TO OUTPUT



RESET TO OUTPUT (DATA HIGH)

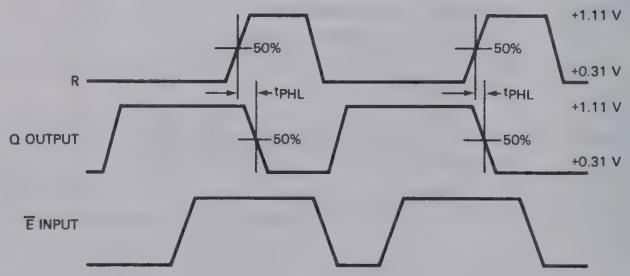


Fig. 1.

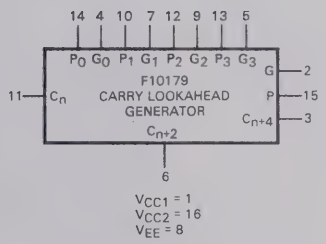
F10179
CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The F10179 is a high speed carry generator intended for use with the F10181 4-bit ALU. Typical addition times for two 32-bit words is 30 ns when using F10181 in the ripple carry mode. When the F10179 carry lookahead generator is used, the typical add time drops to 18 ns.

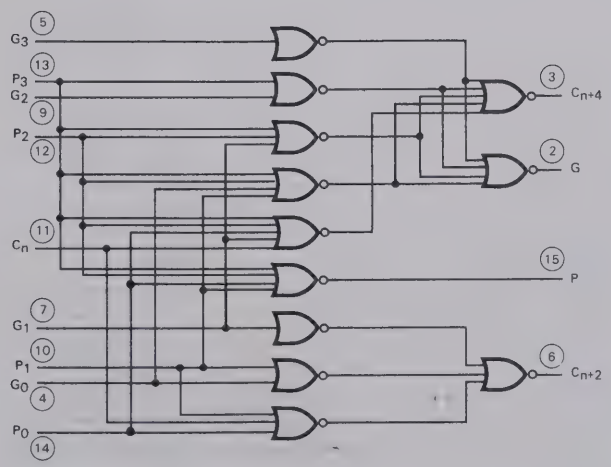
LEAD NAMES

C_n	Carry In
$C_{n+2, +4}$	Carry Out
P	Propagate
G	Generate

LOGIC SYMBOL



LOGIC DIAGRAM



$P = P_0 + P_1 + P_2 + P_3$

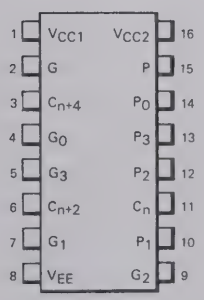
○ = LEAD NUMBERS

$G = (G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)\,G_3$

$C_{n+2} = (C_n + P_0 + P_1)(G_0 + P_1)\,G_1$

$C_{n+4} = (C_n + P_0 + P_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)\,G_3$

CONNECTION DIAGRAM
DIP (TOP VIEW)



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$C_{n+2} = G_1 (G_0 + P_1) (C_n + P_1 + P_0)$ (Product of Max terms)

or

$C_{n+2} = \overline{G}_1 + \overline{G}_0 \overline{P}_1 + \overline{C}_n \overline{P}_1 \overline{P}_0$ (Complement of the sum of Min terms)

$C_{n+4} = G_3 (G_2 + P_3) (G_1 + P_2 + P_3) (G_0 + P_1 + P_2 + P_3) (C_n + P_0 + P_1 + P_2 + P_3)$

or

$C_{n+4} = \overline{G}_3 + \overline{G}_2 \overline{P}_3 + \overline{G}_1 \overline{P}_2 \overline{P}_3 + \overline{G}_0 \overline{P}_1 \overline{P}_2 \overline{P}_3 + \overline{C}_n \overline{P}_0 \overline{P}_1 \overline{P}_2 \overline{P}_3$

$G_G = G_3 (G_2 + P_3) (G_1 + P_2 + P_3) (G_0 + P_1 + P_2 + P_3)$

or

$G_G = \overline{G}_3 + \overline{G}_2 \overline{P}_3 + \overline{G}_1 \overline{P}_2 \overline{P}_3 + \overline{G}_0 \overline{P}_1 \overline{P}_2 \overline{P}_3$

$P_G = P_0 + P_1 + P_2 + P_3$

or

$P_G = \overline{P}_0 \overline{P}_1 \overline{P}_2 \overline{P}_3$

TRUTH TABLE

INPUTS									OUTPUTS			
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+2}	C_{n+4}	G_G	P_G
X	X	X	H	H					H			
H	H	X	H	X					H			
X	H	H	H	X					H			
X	X	X	L	X					L			
X	L	X	X	L					L			
L	X	L	X	L					L			
X	X	X	X	X	X	X	H	H		H		
X	X	X	X	X	H	H	H	X		H		
X	X	X	H	H	H	X	H	X		H		
X	H	H	H	X	H	X	H	X		H		
H	H	X	H	X	H	X	H	X		H		
X	X	X	X	X	X	X	L	X		L		
X	X	X	X	X	L	X	X	L		L		
X	X	X	L	X	X	L	X	L		L		
X	L	X	X	L	X	L	X	L		L		
L	X	L	X	L	X	L	X	L		L		
	X		X	X	X	X	H	H			H	
	X		X	X	H	H	H	X			H	
	X		H	H	H	X	H	X			H	
	H		H	X	H	X	H	X			H	
	X		X	X	X	X	L				L	
	X		X	X	L	X	X	L			L	
	X		L	X	X	L	X	L			L	
	L		X	L	X	L	X	L			L	
		H		X		X		X				H
		X		H		X		X				H
		X		X		H		X				H
		X		X		X		H				H
		L		L		L		L				L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

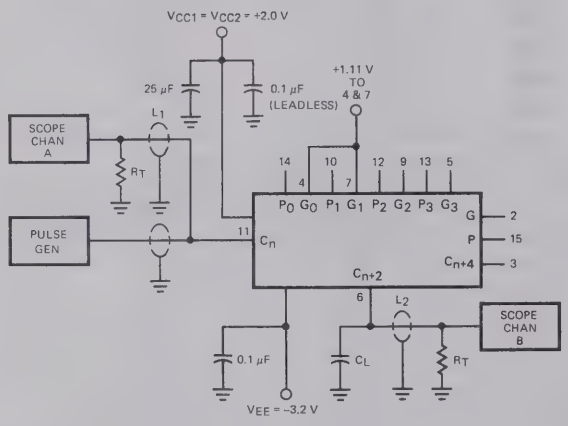
DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND

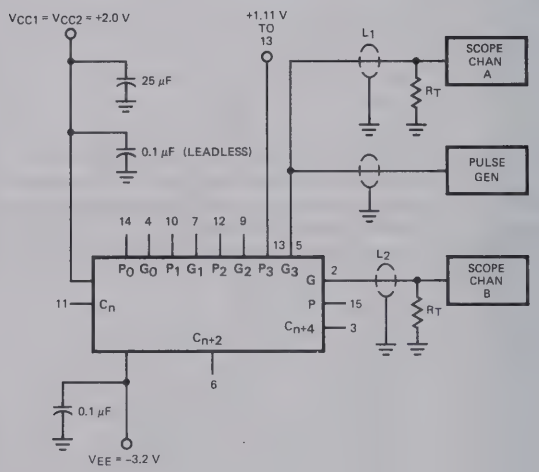
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS		
V_{OH}	Output Voltage HIGH	–1000 –960 –900		–840 –810 –720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	
V_{OL}	Output Voltage LOW C_{n+4} and C_{n+2}	–2000 –1990 –1930		–1665 –1650 –1625	mV	0°C 25°C 75°C		
V_{OL}	Output Voltage LOW G and P	–1870 –1850 –1830		–1665 –1650 –1625	mV	0°C 25°C 75°C		Loading is 50 Ω to –2.0 V
V_{OHC}	Output Voltage HIGH	–1020 –980 –920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1645 –1630 –1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	–1145 –1105 –1045		–840 –810 –720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1870 –1850 –1830		–1490 –1475 –1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH G_0, G_1, C_n G_2, G_3 P_0 P_1, P_3 P_2			 270 225 355 440 395	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	–72	–59		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay LOW to HIGH C_n to C_{n+2}	1.0	3.0	4.5	ns	See Figure 1
t_{PHL}	Propagation Delay HIGH to LOW C_n to C_{n+2}	1.0	3.0	4.5	ns	
t_{PLH}	Propagation Delay LOW to HIGH G_3 to G	1.0	4.0	5.5	ns	See Figure 2
t_{PHL}	Propagation Delay HIGH to LOW G_3 to G	1.0	4.0	5.5	ns	
t_{TLH}	Output Transition Time LOW to HIGH C_n (20%–80%)	0.8	3.5	5.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW C_n (80%–20%)	0.8	3.5	5.5	ns	

SWITCHING CIRCUITS AND WAVEFORMS





L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
V_{CC1} = V_{CC2} = 2.0 V
V_{EE} = -3.2 V

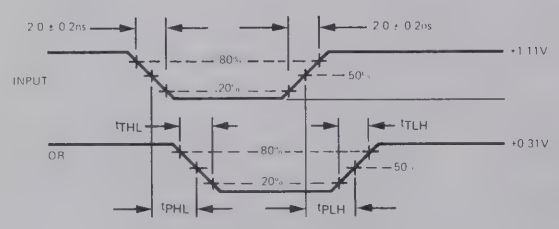


Fig. 1. For Output 6

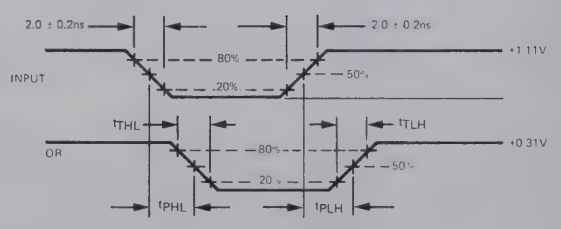


Fig. 2. For Output 2

F10405

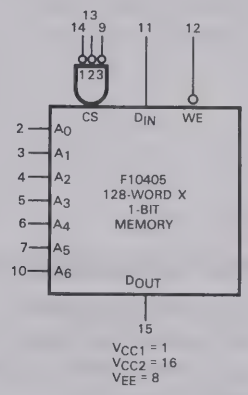
128×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

GENERAL DESCRIPTION — The F10405 is an ECL Read/Write Random Access Memory, organized 128 words by one bit. It has a typical access time of 12 ns and is designed for high speed scratch pad, control and buffer storage applications. It is fully compatible with F10K voltage compensated ECL and conventional 10,000 ECL.

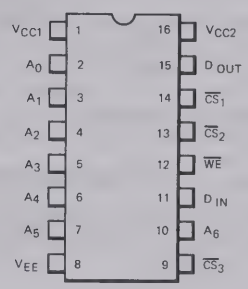
The F10405 has full address decoding on chip, separate data in and non-inverted data out lines and three active LOW chip select lines.

- **FULLY COMPATIBLE WITH F10K AND CONVENTIONAL 10K ECL**
- **READ ACCESS TIME — 11 ns TYP**
- **50 kΩ INPUT PULL DOWN RESISTORS ON CHIP SELECT**
- **ORGANIZED 128 WORDS x 1 BIT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **CHIP SELECT ACCESS TIME — 5 ns TYP**

LOGIC SYMBOL



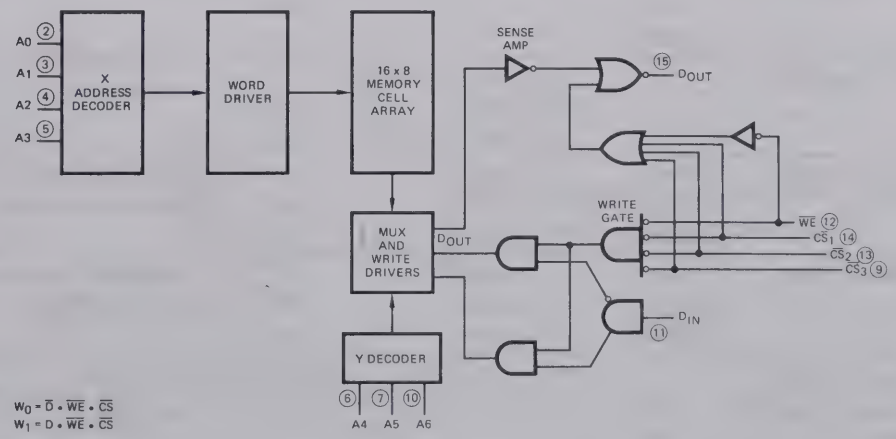
CONNECTION DIAGRAM
DIP (TOP VIEW)



LEAD NAMES

$\overline{CS}_n$	Chip Select Inputs
A_n	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC BLOCK



$W_0 = \overline{D} \cdot \overline{WE} \cdot \overline{CS}$
$W_1 = D \cdot \overline{WE} \cdot \overline{CS}$

◯ = LEAD NUMBERS

7

FUNCTIONAL DESCRIPTION — The F10405 is a fully decoded Read/Write Random Access ECL Memory, organized 128 words by 1 bit. The desired word is selected by a 7-bit address A_0 to A_6.

The chip selects and write enable are active LOW. Three chip selects are provided for memory expansion. This permits memory array expansion up to 1024 words with the 9538 decoder. For larger memories, the third chip select line permits the decoding of Chip Select, CS, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (lead 12). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To Read, $\overline{WE}$ is held HIGH, and the chip is selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH. A write operation may be performed with the write pulse applied to one of the chip select inputs. The two other chip selects and the write enable must be LOW.

Open emitter outputs are provided on the F10405 to allow maximum flexibility in output wired-OR connections for memory expansion.

TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	D_{OUT}	Read

NOTE:

LOW = –1.6 V
HIGH = –0.8 V
(Nominal Values)

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Lead Potential to Ground Lead	+0.5 V to –7.0 V
Input Voltage (dc)	+0.5 V to V_{EE}
Output Current (dc Output HIGH)	+30 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to +75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND (Notes 1-4)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6)			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		Loading is 50 Ω to –2.0 V
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			200	μA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}_n$	0.5		160	μA	+25°C	V_{IN} = V_{ILB}	
	All others	–50			μA			
I_{EE}	Power Supply Current		–90		mA	+25°C	Inputs and Output Open	

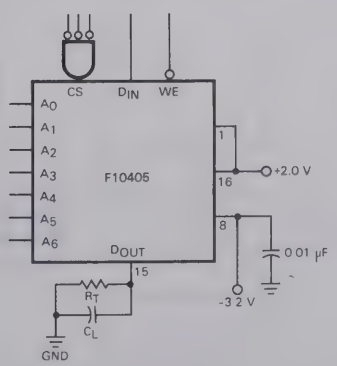
AC CHARACTERISTICS: V_{EE} = –5.2 V ±5%, Output Load = 50 Ω, 10 pF to –2.0 V, T_A = 0°C to +75°C (Note 4)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP Note 7	LIMITS MAX	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		5	8	ns	Fig. 2a & b Measured at 50%
t_{RCS}	Chip Select Recovery Time		5	8	ns	of Input to 50% of Output
t_{AA}	Address Access Time (Note 5)		11	15	ns	
WRITE MODE						
t_W	Write Pulse Width	8	6		ns	t_{WSA} = 4 ns
t_{WSD}	Data Set-up Time Prior to Write	4	3		ns	
t_{WHD}	Data Hold Time After Write	3	0		ns	t_W = 8 ns Fig. 3 Measured at 50% of
t_{WSA}	Address Set-up Time	4	3		ns	Input to 50% of Output.
t_{WHA}	Address Hold Time	3	2		ns	
t_{WSCS}	Chip Select Set-up Time	4	3		ns	
t_{WHCS}	Chip Select Hold Time	3	2		ns	
t_{WS}	Write Disable Time		6	9	ns	
t_{WR}	Write Recovery Time		6	10	ns	
RISE AND FALL TIME						
t_r	Output Rise Time		3		ns	Measured between 20% &
t_f	Output Fall Time		3		ns	80% points. (Fig. 2a)
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	
C_{OUT}	Output Lead Capacitance		7	8	pF	

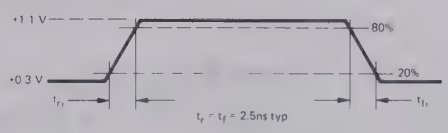
NOTES:
1. Conditions for testing not shown in the tables are chosen to guarantee operation under worst case conditions.
2. The specified LIMITS represent the worst case value for the parameter. Since these worst case values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{EE} = –5.2 V, +25°C, and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F. P. M. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/W (still air)
   θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F. P. M. air flow)
   θ_{JC} (Junction to Case) = 25°C/W
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

SWITCHING TEST CIRCUIT AND WAVEFORM

TESTING CONDITIONS



INPUT LEVELS



All timing measurements referenced to 50% of input levels.

C_L = 10 pF including jig and stray capacitance
R_T = 50 Ω termination of scope

Fig. 1

WAVEFORMS (Cont'd.)

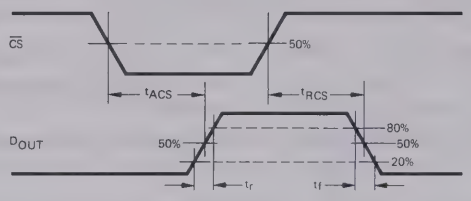


Fig. 2a. Read Mode Propagation Delay from Chip Select

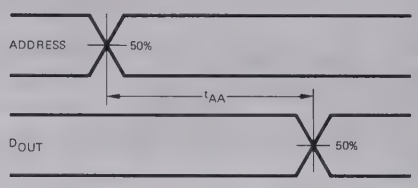


Fig. 2b. Read Mode Propagation Delay from Address

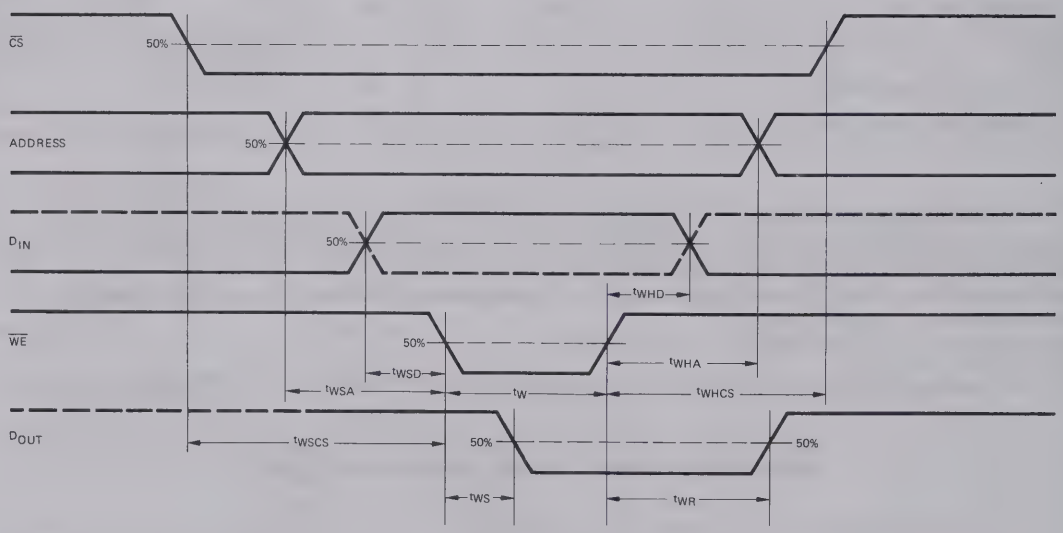


Fig. 3. Write Mode

F10410

256×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

GENERAL DESCRIPTION — The F10410 is a 256-Bit Read/Write Random Access Memory, organized 256 words x 1-bit. It has typical access time of 20 ns and is designed for high speed scratch pad, control and buffer storage applications.

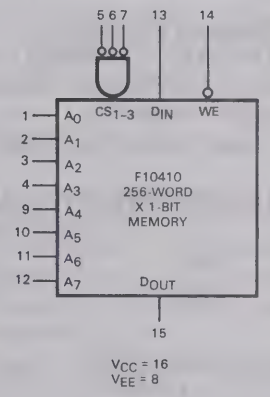
The F10410 includes full address decoding on the chip, has separate date in and non-inverted data out lines, and has three active LOW chip select lines.

- **COMPATIBLE WITH F10K AND CONVENTIONAL 10K ECL LOGIC**
- **READ ACCESS TIME — 20 ns TYP**
- **CHIP SELECT ACCESS TIME — 7 ns TYP**
- **POWER DISSIPATION — 1.8 mW/BIT**
- **50 kΩ INPUT PULL DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

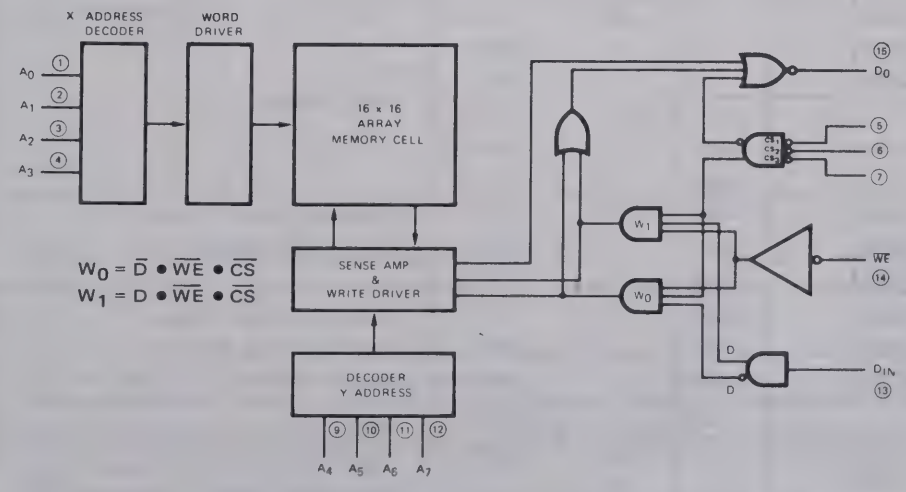
LEAD NAMES

$\overline{CS}_n$	Chip Select Inputs
A_n	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

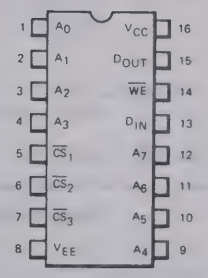
LOGIC SYMBOL



BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION — The F10410 is a fully decoded 256-Bit Read/Write Random Access Memory, organized 256 words by 1 bit. Bit selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW chip select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (lead 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10410 to allow maximum flexibility in output wired-OR connection for memory expansion.

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Lead Potential to Ground Lead	+0.5 V to –6.0 V
Input Voltage (dc)	+0.5 V to V_{EE}
Output Current (dc Output HIGH)	+30 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω to –2.0 V, T_A = 0°C to 75°C (Note 4)

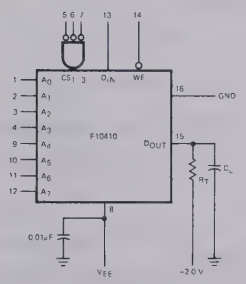
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS		
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}_n$	0.5		170	μA	+25°C	$V_{IN} = V_{ILB}$	
	All others	–50			μA			
I_{EE}	Power Supply Current		–85	–120	mA	+75°C	All Inputs and Outputs Open	
	Lead 8		–95	–130	mA	0°C		

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V ±5%, Output Load = 50 Ω, 30 pF to –2.0 V, T_A = 0°C to 75°C (Note 4)

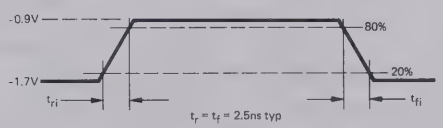
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		7	12	ns	Fig. 2a & b Measured at 50%
t_{RCS}	Chip Select Recovery Time		7	12	ns	of Input to Valid Output
t_{AA}	Address Access Time		20	35	ns	(V_{ILX} for V_{OL} or V_{IHX} for V_{OH}). Note 5.
WRITE MODE						
t_W	Write Pulse Width	25	15		ns	t_{WSA} = 8 ns
t_{WSD}	Data Set-up Time Prior to Write	5	3		ns	
t_{WHD}	Data Hold Time After Write	5	3		ns	
t_{WSA}	Address Set-up Time	8	5		ns	t_W = 25 ns Fig. 3 Measured at 50% of
t_{WHA}	Address Hold Time	2	0		ns	Input to Valid Output
t_{WSCS}	Chip Select Set-up Time	5	3		ns	(V_{ILX} for V_{OL} or
t_{WHCS}	Chip Select Hold Time	5	3		ns	V_{IHX} for V_{OH})
t_{WS}	Write Disable Time	3	14		ns	
t_{WR}	Write Recovery Time		15	20	ns	
RISE AND FALL TIME						
t_r	Output Rise Time		5		ns	Measured between 20% &
t_f	Output Fall Time		5		ns	80% points. (Fig. 2a)
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	
C_{OUT}	Output Lead Capacitance		7	8	pF	

AC TEST CIRCUIT AND WAVEFORMS

TESTING CONDITIONS



INPUT LEVELS



All timing measurements referenced to 50% of input levels.

C_L = 30 pF including jig and stray capacitance
R_T = 50 Ω termination of scope

Fig. 1.

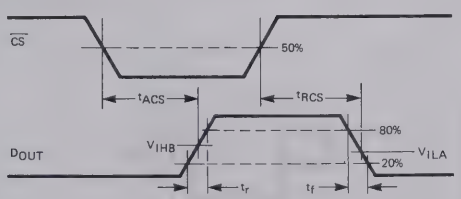


Fig. 2a. Read Mode Propagation Delay from Chip Select

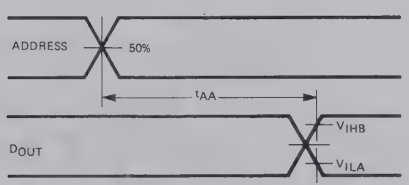


Fig. 2b. Read Mode Propagation Delay from Address

NOTES:

1. Conditions for testing, not shown in the tables are chosen to guarantee operation under worst case conditions.
2. The specified limits represent the worst case value for the parameter. Since these worst case values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{EE} = –5.2 V, TA = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/W (still air)
   θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/W
5. The maximum address access time is guaranteed to be the worse case bit in the memory using a pseudorandom testing pattern.

WAVEFORMS (Cont'd.)

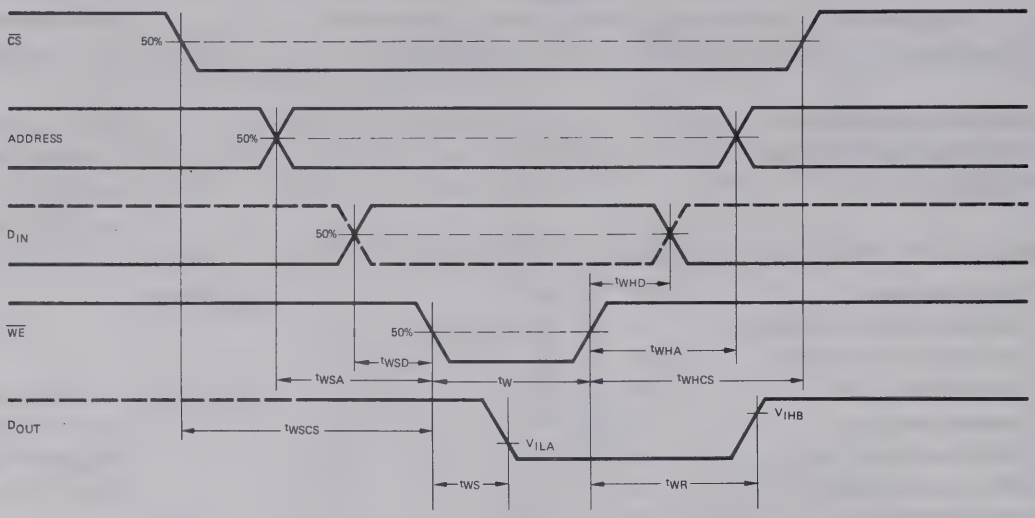


Fig. 3. Write Mode

TYPICAL APPLICATION

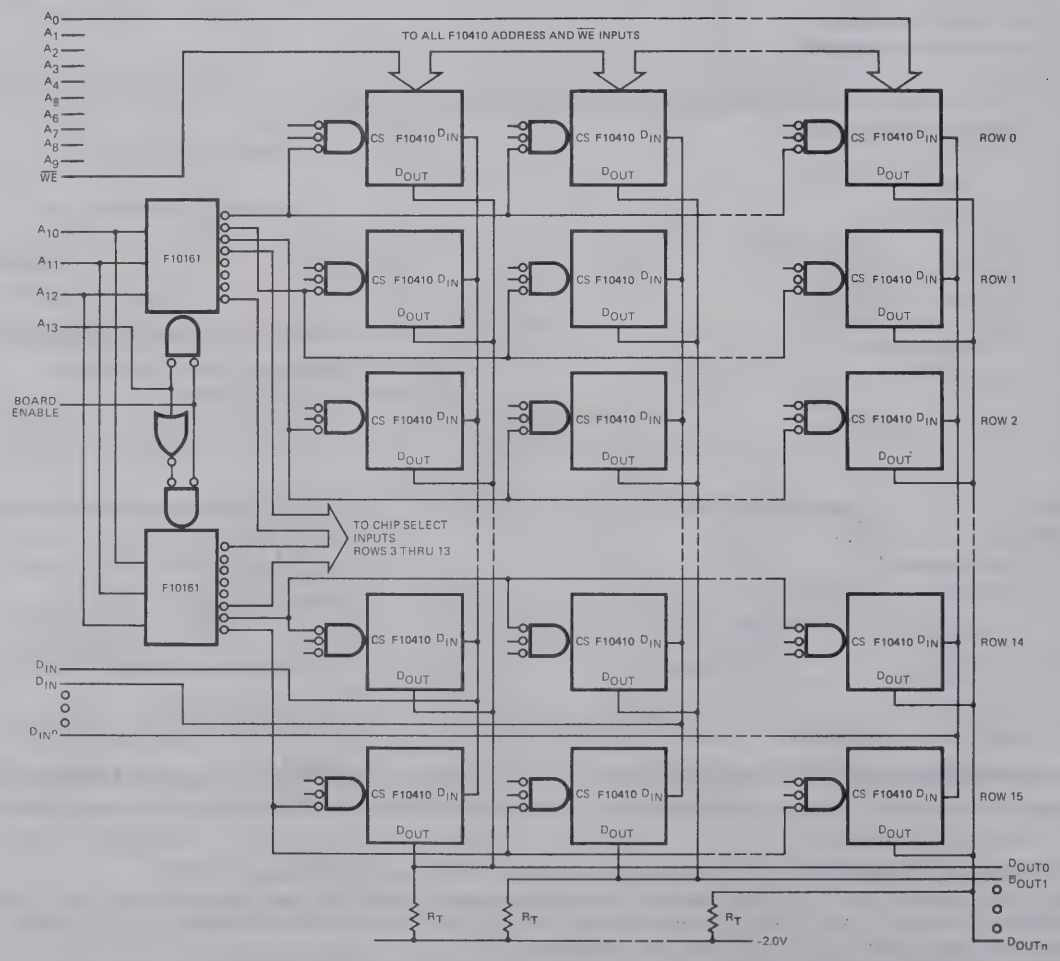


Fig. 4. 4096-Word x n-Bit System

F10415

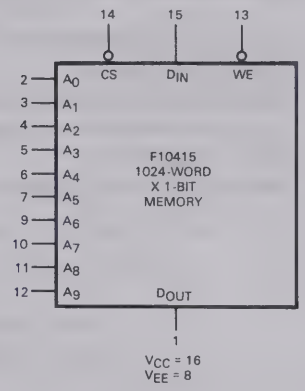
1024×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

GENERAL DESCRIPTION — The F10415 is a 1024-Bit Read/Write Random Access Memory, organized 1024 words x 1-bit. It has typical access time of 45 ns and is designed for high speed scratch pad, control and buffer storage applications.

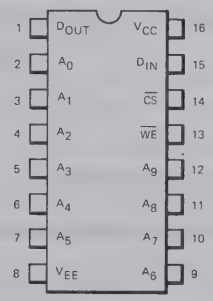
The F10415 includes full address decoding on the chip, has separate data in and non-inverted data out lines, and an active LOW chip select line.

- **FULLY COMPATIBLE WITH F10K AND CONVENTIONAL 10K ECL**
- **READ ACCESS TIME — 45 ns TYP**
- **CHIP SELECT ACCESS TIME — 15 ns TYP**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.5 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

LOGIC SYMBOL



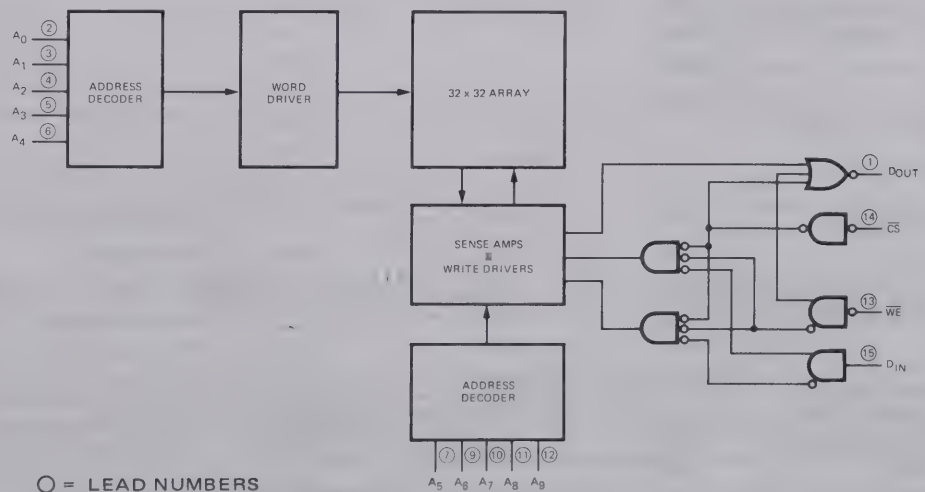
CONNECTION DIAGRAM
DIP (TOP VIEW)



LEAD NAMES

$\overline{CS}$	Chip Select Input
A_n	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

BLOCK DIAGRAM



○ = LEAD NUMBERS

FUNCTIONAL DESCRIPTION — The F10415 is a fully decoded 1024-Bit Read/Write Random Access Memory organized 1024 words by 1 bit. Bit selection is achieved by means of a 10-bit address A_0 to A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for an additional external decoder. For larger memories the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ (lead 13). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter follower output is provided on the F10415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415 can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to –2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Lead Potential to Ground Lead	+0.5 V to –6.0 V
Input Voltage (dc)	+0.5 V to V_{EE}
Output Current (dc Output HIGH)	–30 mA

TRUTH TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	INPUTS D_{IN}	OUTPUT OPEN EMITTER	MODE
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω and 30 pF to –2.0 V, T_A = 0°C to 75°C (Note 4)

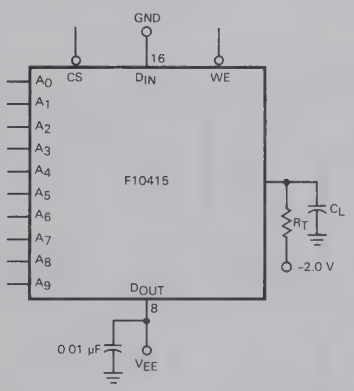
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	+25°C	V_{IN} = V_{ILB}	
	All others	–50			μA			
I_{EE}	Power Supply Current		–90	–125	mA	≥25°C	All Inputs and Outputs Open	
	Lead 8		–100	–150	mA	<25°C		

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V ±5%, Output Load = 50 Ω, 30 pF to –2.0 V, T_A = 0°C to 75°C

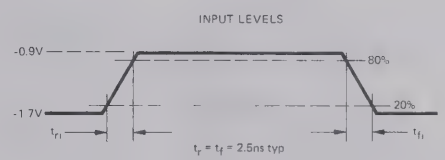
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS
READ MODE						Fig. 2a & b measured at 50%
t_{ACS}	Chip Select Access Time		15	30	ns	of input to valid output
t_{RCS}	Chip Select Recovery Time		20	35	ns	(V_{ILA} mV for V_{OL} or
t_{AA}	Address Access Time		45	65	ns	V_{IHB} for V_{OH})
WRITE MODE						
t_W	Write Pulse Width (to guarantee writing)	40	30		ns	t_{WSA} = 20 ns
t_{WSD}	Data Set-up Time Prior to Write	5	0		ns	
t_{WHD}	Data Hold Time After Write	5	0		ns	Fig. 3 measured
t_{WSA}	Address Set-up Time Prior to Write	20	15		ns	t_W = 40 ns at 50% of input
t_{WHA}	Address Hold Time After Write	5	0		ns	to valid output
t_{WSCS}	Chip Select Set-up Time Prior to Write	5	0		ns	(V_{ILA} for V_{OL} or
t_{WHCS}	Chip Select Hold Time After Write	5	0		ns	V_{IHB} for V_{OH})
t_{WS}	Write Disable Time	30	20		ns	
t_{WR}	Write Recovery Time	30	20		ns	
RISE AND FALL TIME						
t_r	Output Rise Time		5		ns	Measured between 20% and
t_f	Output Fall Time		5		ns	80% points. (Fig. 2a)
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	Measure with a
C_{OUT}	Output Lead Capacitance		7	8	pF	Pulse Technique

SWITCHING TEST CIRCUIT AND WAVEFORMS

TESTING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels.

C_L = 30 pF including jig and stray capacitance
R_T = 50 Ω termination of scope

Fig. 1

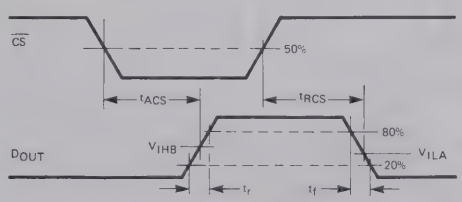


Fig. 2a. Read Mode Propagation Delay from Chip Select

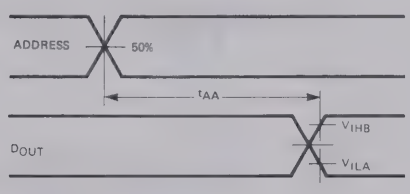


Fig. 2b. Read Mode Propagation Delay from Address

NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under worst case conditions.
2. The specified Limits represent the worst case value for the parameter. Since these worst case values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{EE} = –5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/W (still air)
   θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/W
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

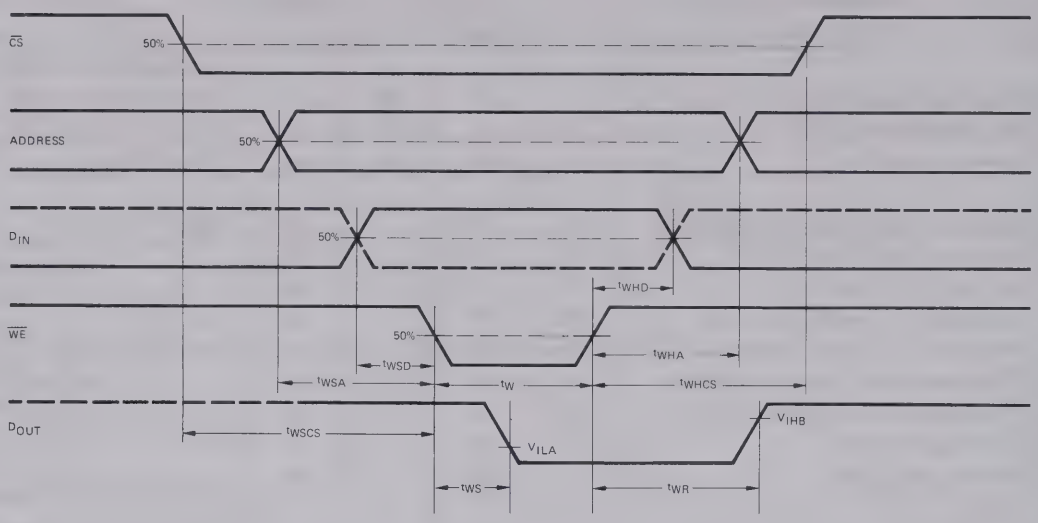


Fig. 3. Write Mode

APPLICATIONS

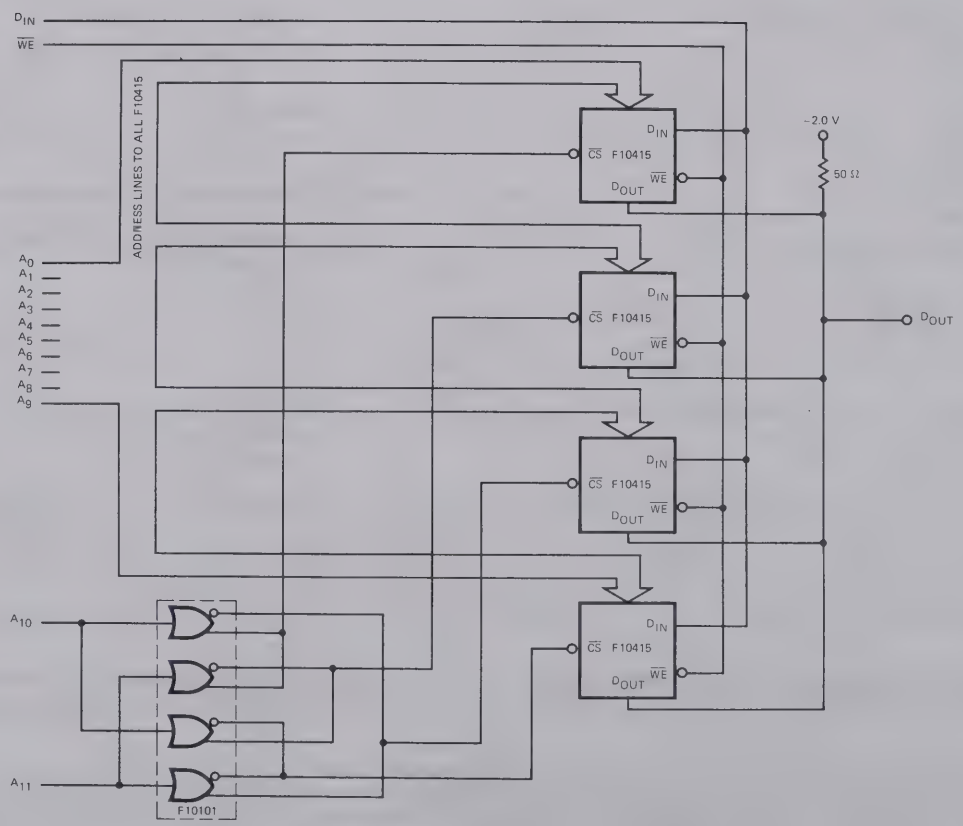


Fig. 4. 4096-Word x 1-Bit System

APPLICATIONS (Cont'd.)

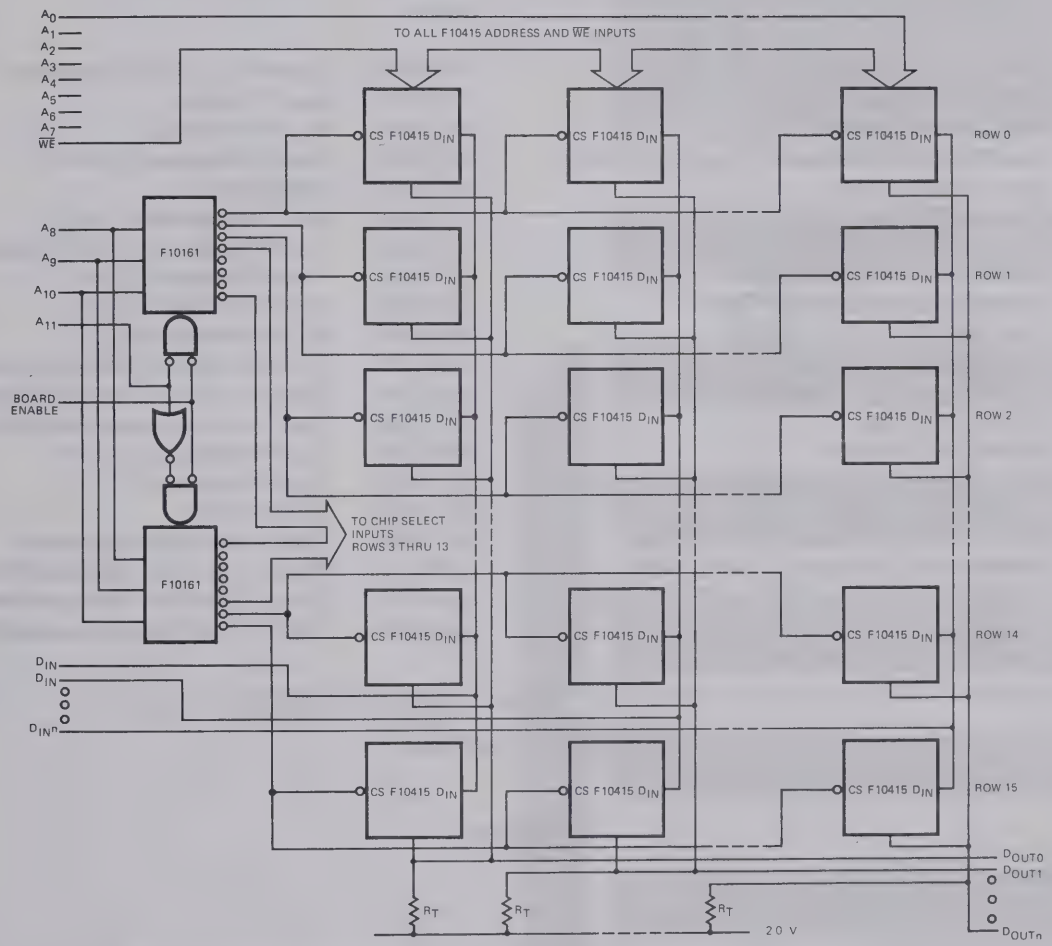
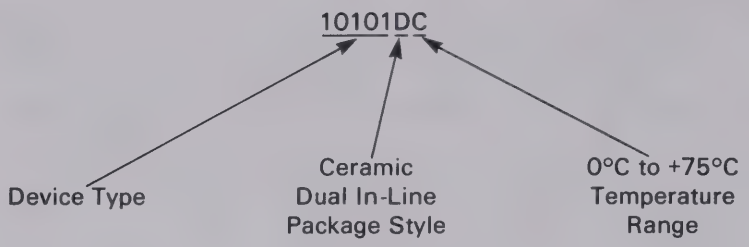


Fig. 5. 16,384-Word x n-Bit System

ORDERING AND PACKAGE INFORMATION

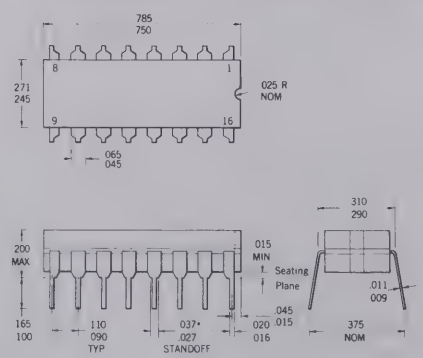
The order code format and correct ordering codes for the products described in these data sheets are as follows:



ORDERING CODE	DESCRIPTION
10000DC	4-Bit Shift Register
10010DC	BCD Decade Counter
10016DC	4-Bit Binary Counter
10101DC	Quad OR/NOR Gate with Common Enable
10102DC	Quad-2 NOR Gate
10103DC	Quad-2 OR Gate
10105DC	Triple 2-3-2-Input OR/NOR Gate
10106DC	Triple 4-3-3-Input NOR Gate
10107DC	Triple Exclusive OR/NOR Gate
10109DC	Dual 4-5-Input OR/NOR Gate
10110DC	Dual 3-Input/3-Output OR Gate
10111DC	Dual 3-Input/3-Output NOR Gate
10115DC	Quad Line Receiver
10116DC	Triple Line Receiver
10117DC	Dual 2-Wide 2-3-Input OR/AND, OR/AND/INVERT Gate
10118DC	Dual 2-Wide 3-3-Input OR/AND Gate
10119DC	4-Wide 4-3-3-3-Input OR/AND Gate
10121DC	4-Wide 3-3-3-3-Input OR/AND, OR/AND/INVERT Gate
10124DC	Quad TTL to ECL Translator
10125DC	Quad ECL to TTL Translator
10130DC	Dual D Latch
10131DC	Dual D Flip-Flop
10132DC	Dual Multiplexer/Latch
10133DC	Quad Latch
10134DC	Dual Multiplexer/Latch
10160DC	12-Bit Parity Checker/Generator
10161DC	1-of-8 Decoder (LOW)
10162DC	1-of-8 Decoder (HIGH)
10164DC	8-Input Multiplexer
10170DC	11-Input Parity Checker/Generator
10171DC	Dual 1-of-4 Decoder/Demultiplexer (LOW)
10172DC	Dual 1-of-4 Decoder/Demultiplexer (HIGH)
10173DC	Quad Multiplexer/Latch
10174DC	Dual Multiplexer
10175DC	Quint Latch
10179DC	Carry Lookahead Generator
10405DC	128 x 1-Bit Fully Decoded RAM
10410DC	256 x 1-Bit Fully Decoded RAM
10415DC	1024 x 1-Bit Fully Decoded RAM

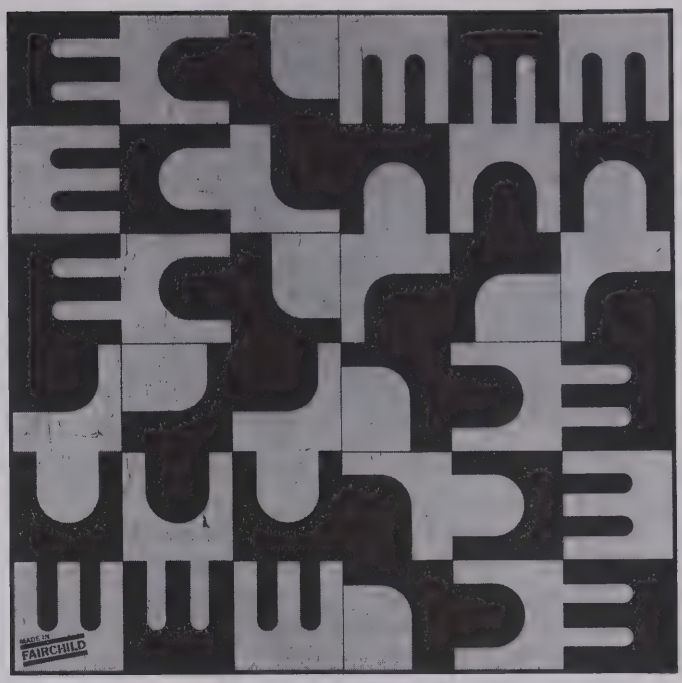
PACKAGE OUTLINE

16-Lead DIP



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
* The .037/.027 dimension does not apply to the corner leads

THE ECL HANDBOOK SECTION SELECTOR



Introduction

ECL USERS GUIDE

ECL for High Performance Systems 1

ECL Circuit Basics 2

ECL Logic Design 3

Transmission Line Concepts 4

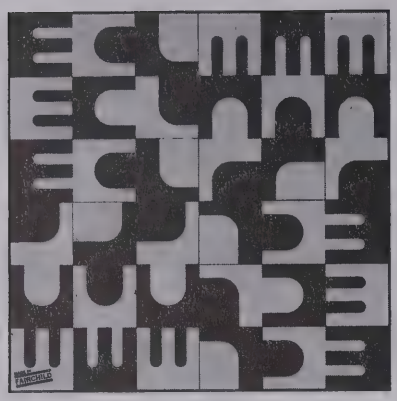
ECL Interconnections 5

Power Distribution and Thermal Considerations 6

ECL PRODUCT INFORMATION

F10K Voltage Compensated ECL Series 7

F95K Fully Compensated ECL Series 8



CHAPTER 8

F95000 4-Bit Shift Register
F95002 Dual 4-Input OR/NOR Gate
F95003 Triple 2-Input OR/NOR Gate
F95004 Quad 2-Input NOR Gate
F95010 BCD Decade Counter
F95016 4-Bit Binary Counter
F95029 Edge-Triggered $J\overline{K}$ Flip-Flop
F95101 Quad OR/NOR Gate with Common Enable
F95102 Quad 2-Input NOR Gate
F95103 Quad 2-Input OR Gate
F95105 Triple 2-3-2-Input OR/NOR Gate
F95106 Triple 4-3-3-Input NOR Gate
F95107 Triple Exclusive OR/NOR Gate
F95109 Dual 4-5-Input OR/NOR Gate
F95110 Dual 3-Input/3-Output OR Gate
F95111 Dual 3-Input/3-Output NOR Gate
F95115 Quad Line Receiver
F95116 Triple Line Receiver
F95124 Quad TTL to ECL Translator
F95130 Dual D Latch
F95231 High Speed Dual D Flip-Flop

F95K FULLY COMPENSATED ECL SERIES

GENERAL DESCRIPTION — Fairchild F95K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

The fully compensated F95K logic elements employ unique compensation networks which ensure that significant parameters such as logic levels, noise margin and propagation delay remain constant over a wide range of temperature and power supply variations.

The 95K series elements have the same lead assignments and logic functions as their 10,000 series counterparts, allowing either selective substitution of F95K elements to eliminate problems in thermal hot-spots or total substitution to upgrade overall system performance.

The series employs Emitter Coupled Logic to achieve typical gate delays of 2 ns at typical power levels of 25 mW/gate. The nominal power supply is specified as V_{EE} equal to –5.2 V. All devices, however, may be operated over V_{EE} ranges of of –4.7 to –6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a V_{EE} range of –3.5 to –6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

High input impedance (typically 50 kΩ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

In accordance with standard IC practice, commerical F95K devices are specified over 0°C to 75°C temperature range.

- **Very high speed . . . typically 2 ns per gate.**
- **Low power dissipation . . . typically 25 mW per gate.**
- **Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.**
- **Internal 50 kΩ (nominal) input pull down resistors . . . unused inputs may be left open.**
- **Open emitter-follower outputs drive terminated lines.**
- **Separate V_{CC} leads eliminate noise coupling.**
- **Single V_{EE} power supply . . . -4.7 to -6.2 V.**
- **Wired-OR capability.**
- **Complementary, simultaneous outputs.**
- **Temperature compensated . . . logic levels, noise margins and propagation delays remain constant over a wide range of temperature variations and gradients.**
- **Simplified customer and vendor specification and testing . . . air flow and warm-up not required to guarantee proper logic levels.**
- **Lowered cooling cost . . . wide temperature gradients between devices does not affect logic levels and noise margin.**

RECOMMENDED OPERATING AND TEST CONDITIONS — The Fairchild F95K series operates in both still or forced air systems where an ambient temperature of 0°C to 75°C is maintained. The required cooling is determined solely by this ambient temperature requirement. There is no need to maintain a constant temperature throughout the system.

The required system voltage at V_{EE} leads is –4.7 to –6.2 V. With a load on all outputs of 50Ω to –2.0 V and a 0°C to a 75°C temperature range, the device dc parameters are guaranteed for a nominal V_{EE} of –5.2 V. With the same operation conditions, the worst case dc parameters are guaranteed for any V_{EE} value from –4.7 to –6.2 V.

The F95K ac switching characteristics are guaranteed at V_{EE} = –5.2 V over the operating ambient temperature range of 0°C to 75°C. The ac test parameters shown use a 50Ω load to –2.0 V.

Since the F95K devices are relatively insensitive to variations in junction temperature, testing may be performed on almost any available digital integrated circuit tester. No power warm-up or moving air cooling is required to assure the specified device characteristics.

ABSOLUTE MAXIMUM RATINGS
(Non-operating, above which useful life may be impaired)

Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–8 V
Input Voltage	Gnd to V_{EE}
Output Current	–50 mA

FUNCTIONAL DESCRIPTION

F95K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1.*

If the input voltages are more negative than V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than V_{BB}, Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

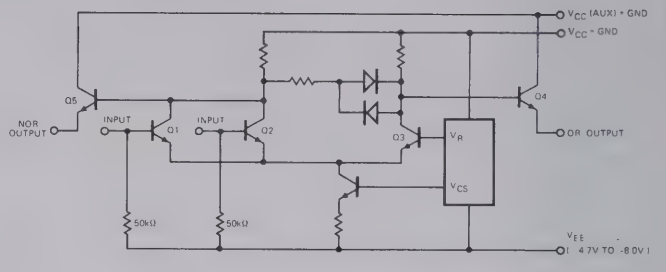


Fig. 1.

TYPICAL ECL TRANSFER CHARACTERISTICS WITH SPECIFICATION POINTS

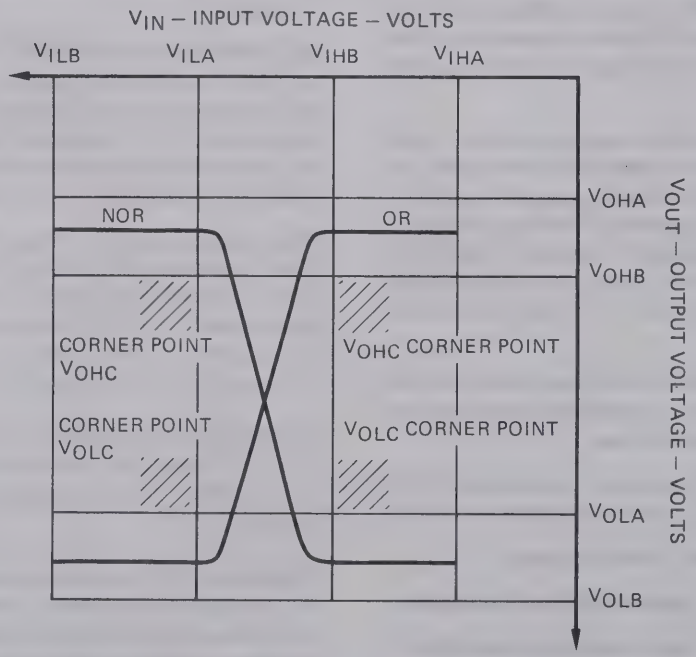
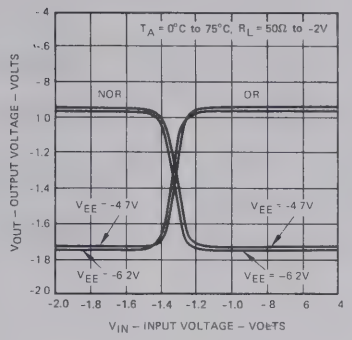


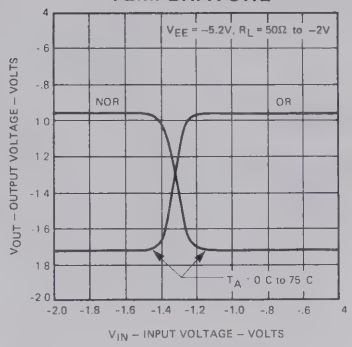
Fig. 2.

TYPICAL F95K SERIES CHARACTERISTICS

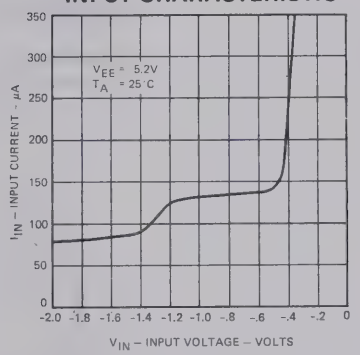
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



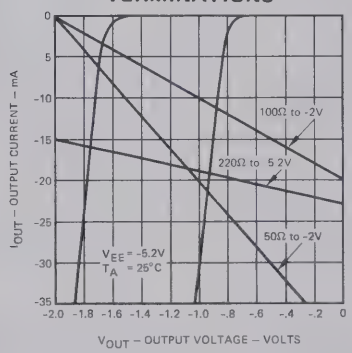
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



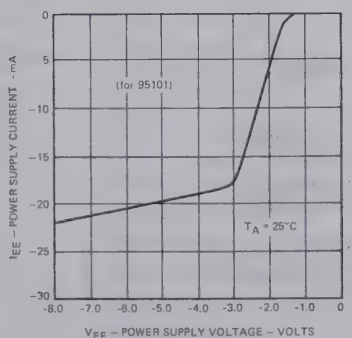
INPUT CHARACTERISTIC



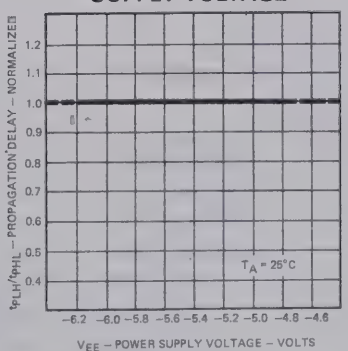
OUTPUT CHARACTERISTICS VERSUS TYPICAL OUTPUT TERMINATIONS



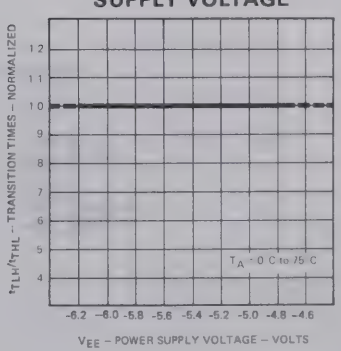
CHANGE IN POWER SUPPLY CURRENT WITH RESPECT TO CHANGE IN POWER SUPPLY VOLTAGE



PROPAGATION DELAY VARIATION VERSUS SUPPLY VOLTAGE



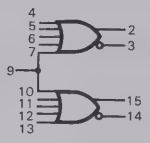
OUTPUT TRANSITION TIME VARIATION VERSUS SUPPLY VOLTAGE



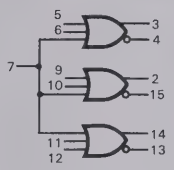
LOGIC DIAGRAMS

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

F95002



F95003



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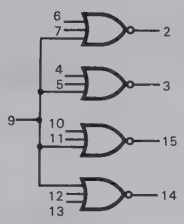
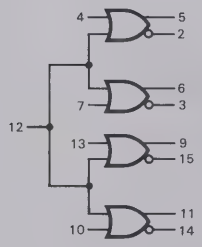
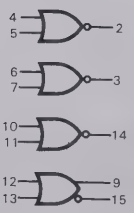


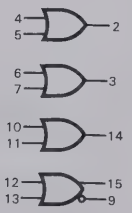
F95101



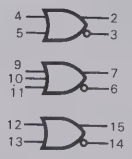
F95102



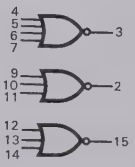
F95103



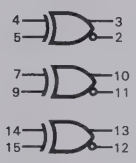
F95105



F95106



F95107

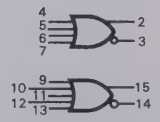


Logic Equation

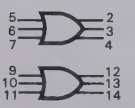
$2 = 4 \cdot \overline{5} + \overline{4} \cdot 5$

$3 = 4 \cdot 5 + \overline{4} \cdot \overline{5}$

F95109

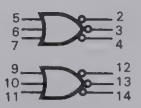


F95110



NOTE: V_{CC1} = 1
V_{CC2} = 15

F95111



NOTE: V_{CC1} = 1
V_{CC2} = 15

F95002 • F95003 • F95004 • F95101 • F95102 • F95103 • F95105 • F95106 • F95107 • F95109 • F95110 F95111

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB} per Logic Function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			260	µA	$V_{IN} = V_{IHA}$	
	F95002 Lead 9			345			
	F95003 Lead 7			430			
	F95004 Lead 9			550			
	F95101 Lead 12			550			
	F95110,F95111 All Inputs			430			
I_{IL}	Input Current LOW	0.5			µA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current				mA	Inputs & Outputs Open	
	F95002,F95109	-14	-10				
	F95003,F95105,F95106	-21	-15				
	F95004,F95101,F95102,F95103	-26	-18				
	F95107	-28	-19				
	F95110,F95111	-35	-25				

DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OHC}	Output Voltage HIGH	-1050			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	Loading is 50Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current				mA	Inputs & Outputs Open V_{EE} = -6.2 V	
	F95002,F95109	-15	-11				
	F95003,F95105,F95106	-22.5	-16				
	F95004,F95101,F95102,F95103	-27.5	-19				
	F95107	-30	-21				
	F95110,F95111	-38	-28				

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 0°C to 75°C **F95002 • F95003 • F95004 • F95101 F95102 • F95103 • F95105 • F95106**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	2.0	3.1	ns	See Figure 1.
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	2.0	3.1	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.6	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.6	ns	

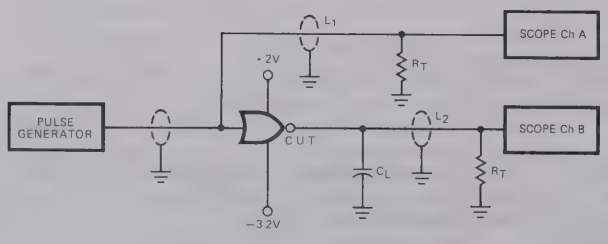
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C **F95107**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay LOW to HIGH	1.1	2.5	4.0	ns	See Figure 1.
t_{PHL}	Propagation Delay HIGH to LOW	1.1	2.5	4.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.8	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.8	ns	

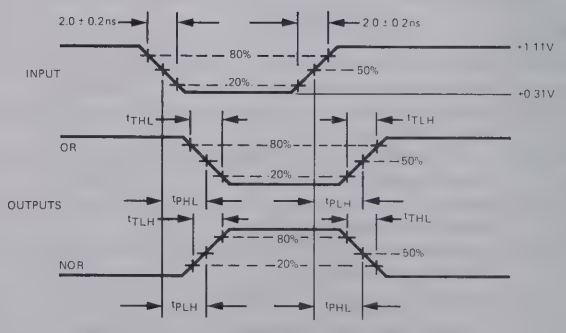
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C **F95110 • F95111**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay LOW to HIGH	1.4	2.5	3.8	ns	See Figure 1.
t_{PHL}	Propagation Delay HIGH to LOW	1.4	2.4	3.8	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.8	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.8	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

Fig. 1.

F95000

4-BIT SHIFT REGISTER

GENERAL DESCRIPTION — The F95000 is a 4-Bit Parallel/Serial In, Parallel/Serial Out Shift Register. High Speed ECL technology permits storage, shifting, counting and serial code conversion at rates in excess of 200 MHz.

Features include assertion outputs for each stage, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

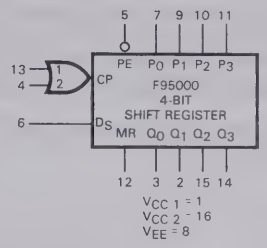
The F95000 incorporates a unique temperature and voltage compensation network which ensures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of temperature and power supply voltage.

- **HIGH SPEED . . . 200 MHz TYPICAL SHIFT FREQUENCY**
- **D TYPE INPUTS SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **TERMINATED LINE DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} LEADS ELIMINATE NOISE COUPLING**
- **50 kΩ INPUT PULL DOWNS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **SINGLE V_{EE} POWER SUPPLY . . . -4.7 V TO -6.2 V**
- **NOISE MARGINS INSENSITIVE TO POWER SUPPLY OR TEMPERATURE VARIATIONS AND GRADIENTS**

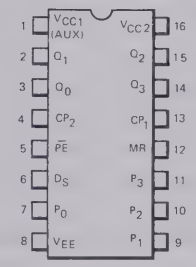
LEAD NAMES

P_n	Parallel Data Inputs
$\overline{PE}$	Parallel Enable (Active LOW)
CP_n	Clock In, Shifts on Positive Transition
MR	Asynchronous Master Reset (Active HIGH)
D_S	Data Input, Serial
Q_n	Register Outputs

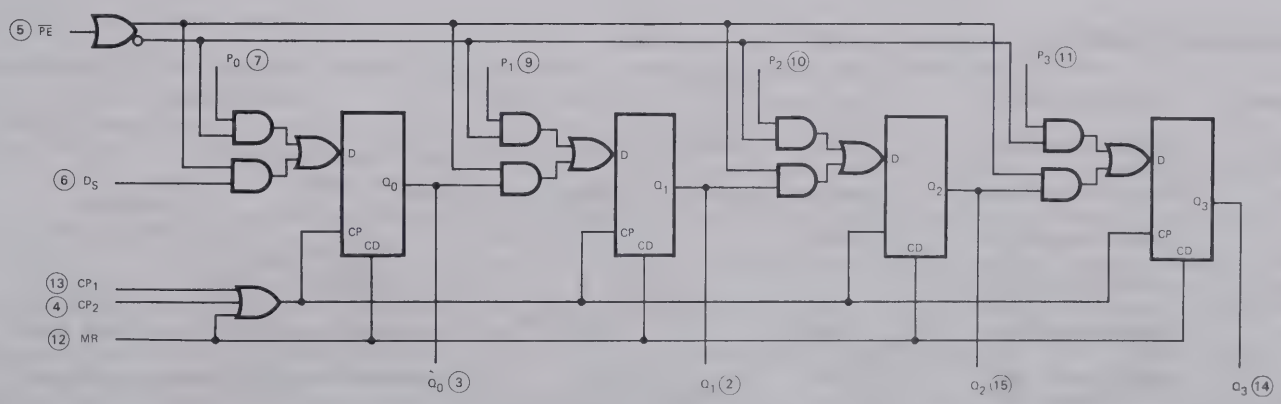
LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



○ = LEAD NUMBERS

Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F95000 is a high speed 4-Bit Shift Register. It consists of four master/slave flip-flops and four 2-input multiplexers interconnected so as to permit loading of the masters from either a preceding slave output (Q_{n-1}) or an external (P_n) input. The function desired is selected by the Parallel Enable ($\overline{PE}$) input.

The masters are loaded during the LOW period of the clock ($CP_{1,2}$). As the clock changes from LOW to HIGH, the masters are inhibited from change followed by the enabling of the data path from master to slave. This data is then presented at the outputs (Q_n). While the clock is HIGH, the masters are inhibited from change and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited. This is followed by the enabling of the masters for the acceptance of data from the parallel or serial logic inputs.

As the two clock inputs ($CP_{1,2}$) are ORed together, both must be LOW for the masters to accept new data. If either is raised to a HIGH, the register is clocked.

A HIGH on one clock input can prevent the register from shifting, providing a hold condition. To prevent false triggering, this input must change from LOW to HIGH while the clock is HIGH.

The Master Reset (MR) function is asynchronous. When held HIGH, it overrides all other commands and forces all outputs (Q_n) LOW.

TRUTH TABLES

MODE SELECT

MR	$\overline{PE}$	CP_1	CP_2	MODE
H	X	X	X	RESET (ALL OUTPUTS LOW)
L	L	L	⌐	PARALLEL LOAD
L	L	⌐	L	PARALLEL LOAD
L	H	L	⌐	SHIFT RIGHT (SERIAL LOAD)
L	H	⌐	L	SHIFT RIGHT (SERIAL LOAD)
L	X	H	X	HOLD
L	X	X	H	HOLD

SERIAL LOAD

D_S	$Q_{O(t+1)}$
H	H
L	L

PARALLEL LOAD

P_n	$Q_{n(t+1)}$
H	H
L	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

⌐ = Clock Pulse (LOW to HIGH)

(t+1) = Time after positive going clock transition

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW Voltage for All Inputs	
I_{IH}	Input Current HIGH MR (Lead 12)			260 700	μA	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			μA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-85	-66		mA	Outputs Open, Lead 4 or 13 Tied to V_{IH}	

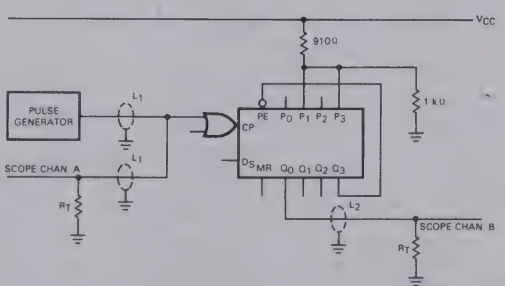
DC CHARACTERISTICS: V_{EE} = –4.7 to –6.2 V, T_A = 0°C to 75°C , V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	–1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW			–1595	mV		
V_{IH}	Input Voltage HIGH	–1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			–1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current		–80		mA	Outputs Open, Lead 4 or 13 Tied to V_{IH} V_{EE} = –6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Shift Right Frequency	150	200		MHz	See Figure 3
t_{PLH}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	See Figure 1
t_{PHL}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		2.5		ns	See Figure 2
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.0	3.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.0	3.5	ns	
t_w	Clock Pulse Width		2.5		ns	See Figure 3
t_w	MR Pulse Width		3.5		ns	
t_s	Set-Up Time Prior to Clock D_S to CP, P_n to CP	1.5	0.5		ns	
t_h	Hold Time After Clock D_S to CP, P_n to CP	1.0	–0.5		ns	
t_s	Set-Up Time Prior to Clock PE to CP	5.4	3.2		ns	
t_h	Hold Time After Clock PE to CP	0	–3.2		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 = L_2 = 50Ω impedence lines
V_{CC} = +2.0 V, leads 1 and 16
V_{EE} = –3.2 V, lead 8
R_T = 50Ω termination of scope
f = 10 MHz
Pulse Width = 10 ns

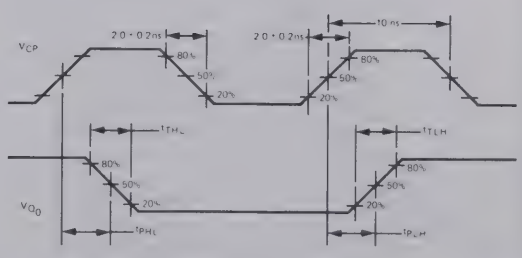
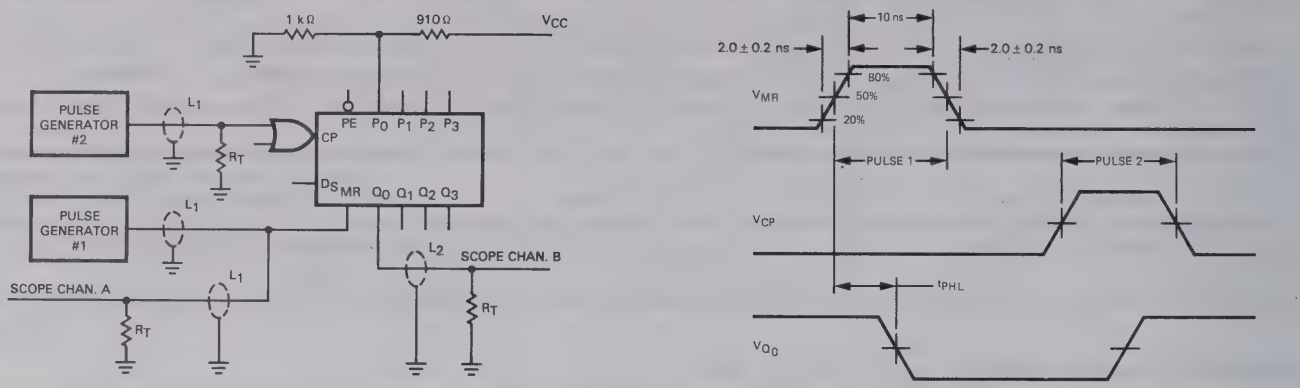


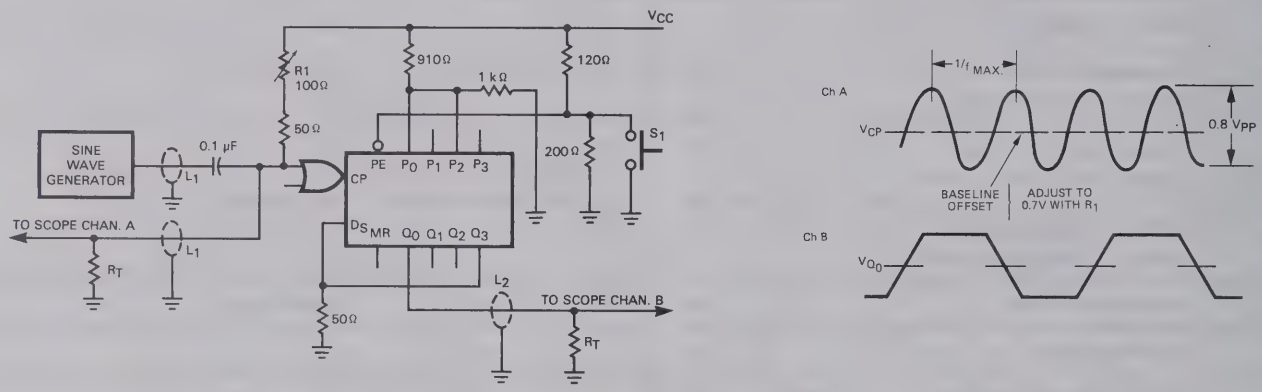
Fig. 1. Clock to Output, Output Transition Time

SWITCHING CIRCUIT AND WAVEFORMS (Cont'd)



$L_1 = L_2 = 50\Omega$ impedance lines.
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\Omega$ termination of scope
f = 10 MHz
Pulse 2 ≃ Pulse 1

Fig. 2. Master Reset to Output

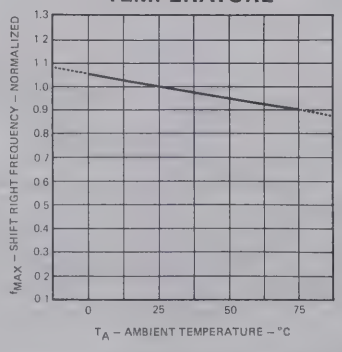


$L_1 = L_2 = 50\Omega$ impedance lines
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\Omega$ termination of scope
$f = f_{MAX}$
Load the register by closing S_1

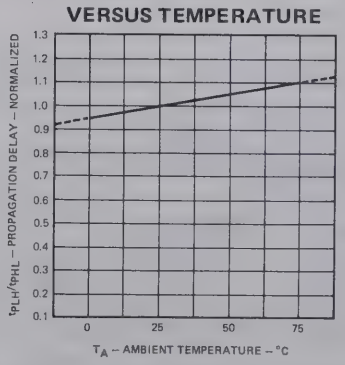
Fig. 3. Shift Frequency

TYPICAL ELECTRICAL CHARACTERISTICS

SHIFT RIGHT FREQUENCY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS TEMPERATURE



F95010 · F95016

BCD DECADE COUNTER/4-BIT BINARY COUNTER

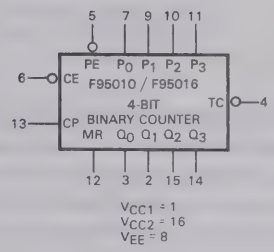
GENERAL DESCRIPTION — The F95010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F95016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 95K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

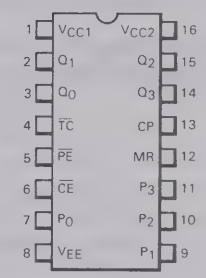
Both devices are packaged in hermetic ceramic 16-lead Dual In-Line packages and are specified for operation over the temperature range 0°C to 75°C.

- **HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY**
- **INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION**
- **ASYNCHRONOUS MASTER RESET**
- **50Ω DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} LEADS — ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL DOWNS**
- **SINGLE -5.2 V POWER SUPPLY**

LOGIC SYMBOL



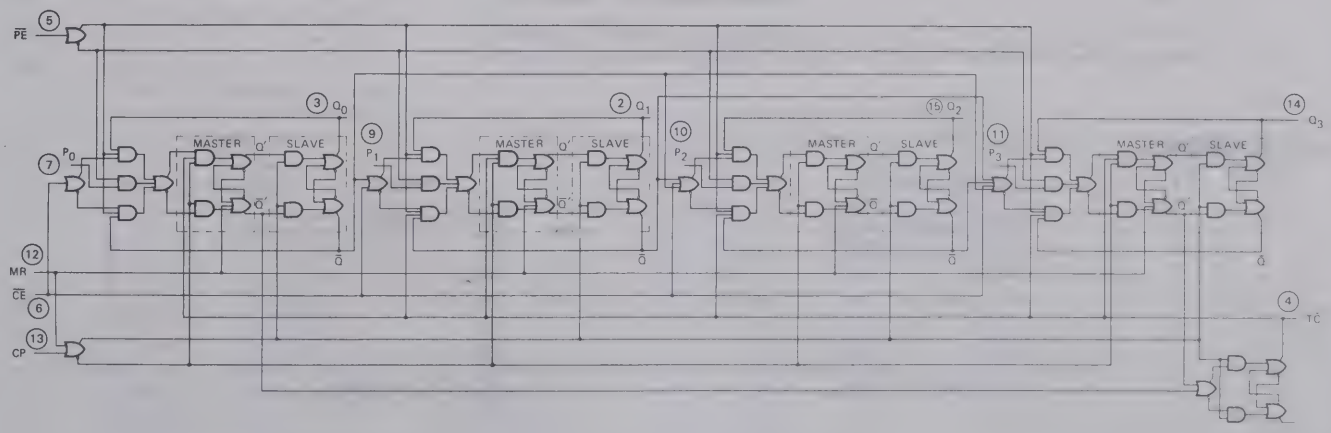
CONNECTION DIAGRAM
DIP (TOP VIEW)



LEAD NAMES

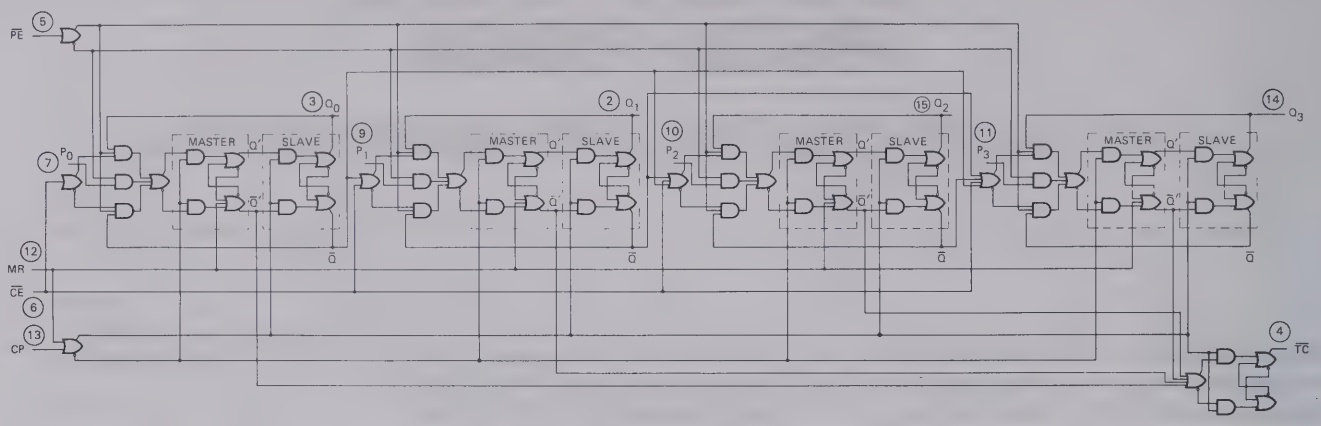
$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (95010, LOW at HLLH; 95016 LOW at HHHH)
Q_n	Counter Outputs

LOGIC DIAGRAM F95010



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC DIAGRAM F95016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F95010 is a high speed BCD Decade Counter and the F95016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 95010 and at count 15 (HHHH) on the 95016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

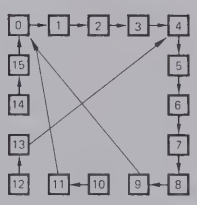
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	⎍	Load Parallel (P_n to Q_n)
H	L	L	⎍	Load Parallel (P_n to Q_n)
L	H	L	⎍	Count
H	H	L	⎍	Hold
X	X	L	⎏	Masters Respond, Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

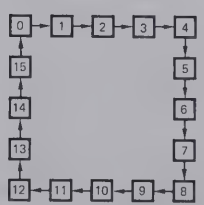
L = LOW
H = HIGH Voltage Level
X = Don't Care
⎍ = Clock Pulse (LOW to HIGH)
⎏ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F95010



F95016



NOTE: The 95010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

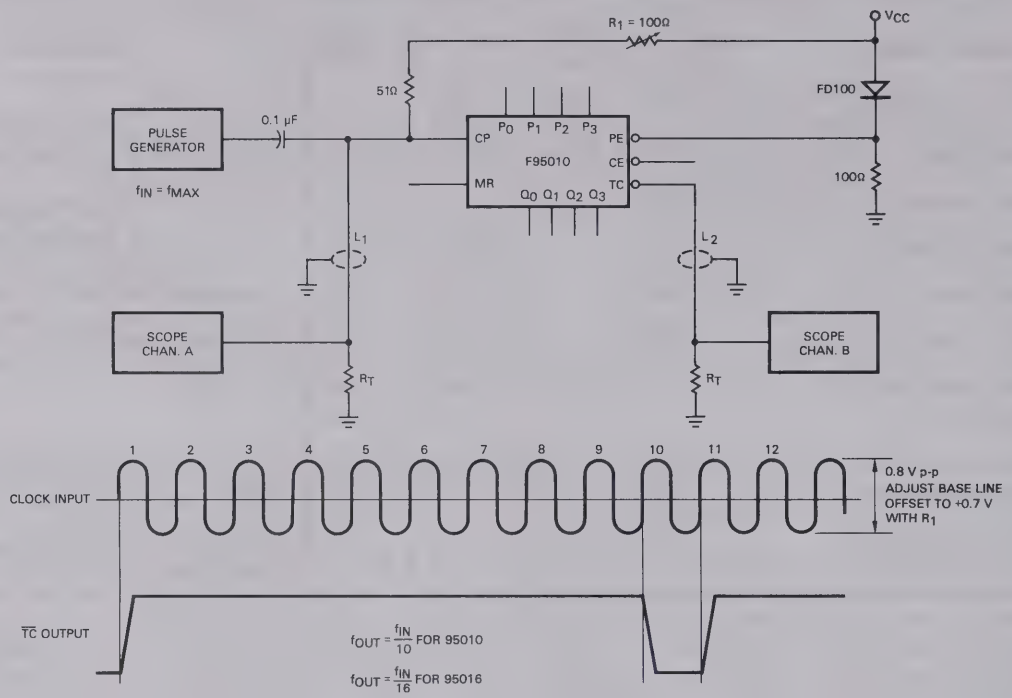
DC ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	50 to -2 V	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV	50 to -2 V	
V_{OHC}	Output Voltage HIGH	-1035			mV	50 to -2 V	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table
V_{OLC}	Output Voltage LOW			-1610	mV	50 to -2 V	
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW for All Inputs	
I_{IH}	Input Current HIGH, MR (Lead 12)			265 700	µA µA	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-115	-80		mA	Outputs Open, Lead 12 to V_{IH}, Other Inputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_h	Hold Time After Clock P_n to CP	1.0			ns	
t_s	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
t_h	Hold Time After Clock PE or CE to CP	0.5			ns	

SWITCHING CIRCUITS AND WAVEFORMS

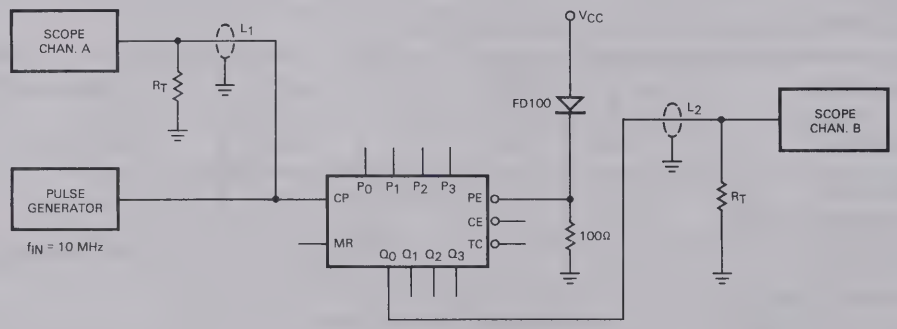


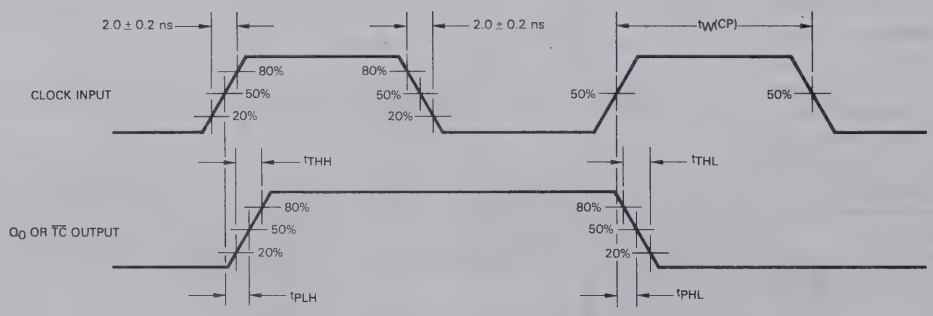
1 2 3 4 5 6 7 8 9 10 11 12
CLOCK INPUT
0.8 V p-p
ADJUST BASE LINE
OFFSET TO +0.7 V
WITH R1
TC OUTPUT
fOUT = fIN/10 FOR 95010
fOUT = fIN/16 FOR 95016

L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency



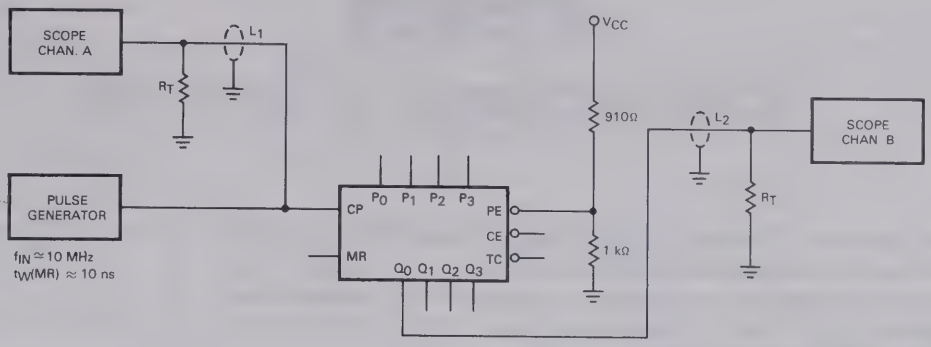


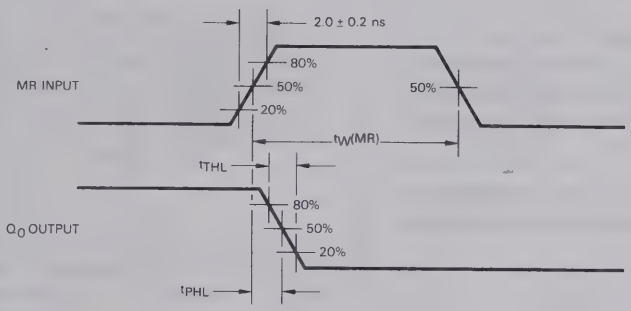
L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Clock to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)



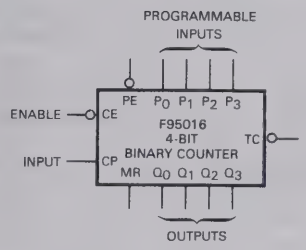


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

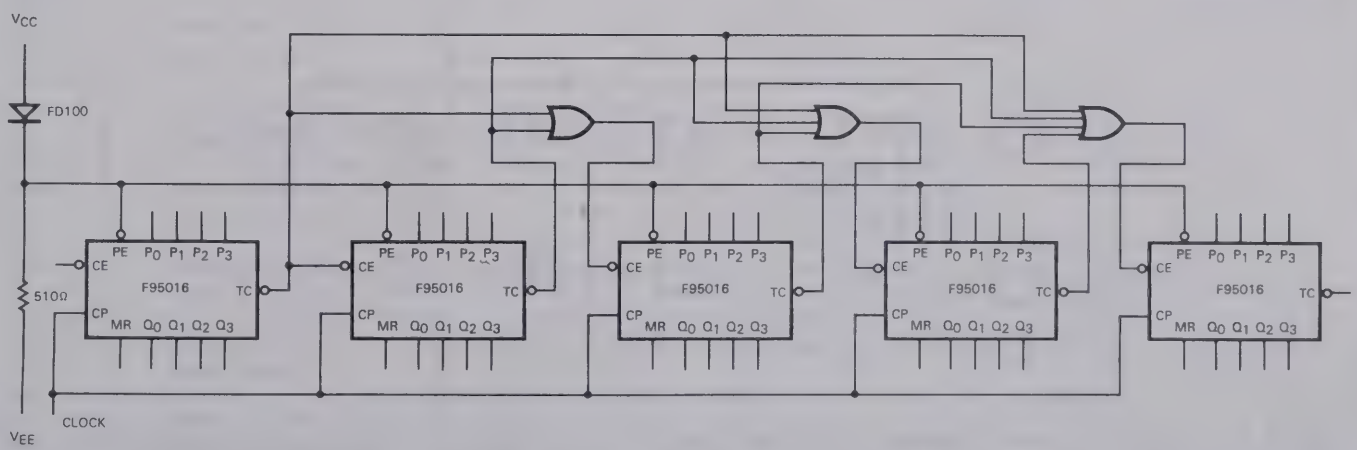
Fig. 3. Master Reset to Output

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F95016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.



CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION

F95029

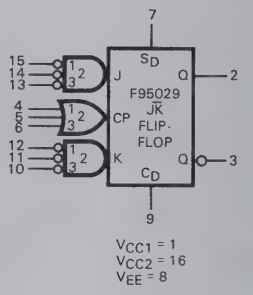
EDGE-TRIGGERED $\overline{J}$ $\overline{K}$ FLIP-FLOP

DESCRIPTION — The F95029 is a very high speed Edge-Triggered $\overline{J}$ $\overline{K}$ Flip-Flop designed for maximum speed. The multiple $\overline{J}$, $\overline{K}$, and clock inputs permit its use in most register and counter applications without extra gates. Careful control of clock pulse rise and fall times is not required, as the master/slave design has a dc threshold on the clock input which initiates the transition on the output.

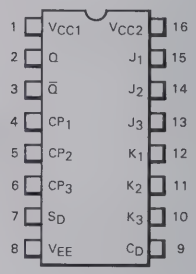
Data is accepted by the master while the clock is LOW. Data present just prior to the rising edge of the clock (as specified by the set-up and hold times) is trapped in the master and transferred to the slave on the rising edge of the clock. Although this device uses a master/slave design, it is not "ones catching" (it responds only to the rising edge of the clock pulse).

The asynchronous inputs provide ability to control the state of the flip-flop independent of the conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided.

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



LEAD NAMES

$\overline{J}$	Synchronous Set Input (Active LOW)
$\overline{K}$	Synchronous Reset Input (Active LOW)
CP	Clock Input
S_D	Asynchronous Set Input
C_D	Asynchronous Clear Input
Q	True Output
$\overline{Q}$	Complement Output

TRUTH TABLES

SYNCHRONOUS

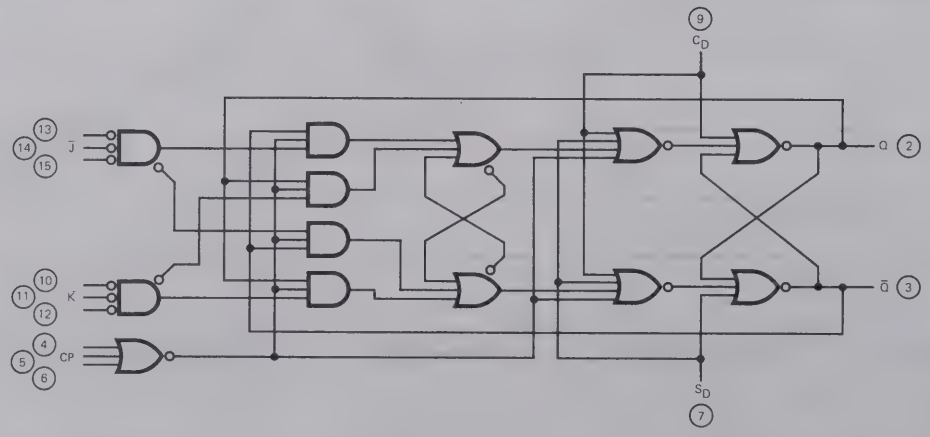
$\overline{J}_1$	$\overline{J}_2$	$\overline{J}_3$	$\overline{K}_1$	$\overline{K}_2$	$\overline{K}_3$	Q_{t+1}
L	L	L	L	L	L	$\overline{Q}_t$
L	L	L	One or More HIGH			H
One or More HIGH			L	L	L	L
One or More HIGH			One or More HIGH			Q_t

ASYNCHRONOUS

C_D	S_D	Q
L	L	Sync
L	H	H
H	L	L
H	H	Undetermined

L = LOW Voltage Level
H = HIGH Voltage Level
Q_t = Present Output State
Q_{t+1} = Output State after next Clock

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	–1025	–965	–880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to –2.0 V
V_{OL}	Output Voltage LOW	–1810	–1705	–1620	mV		
V_{OHC}	Output Voltage HIGH	–1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			–1610	mV		
V_{IH}	Input Voltage HIGH	–1165		–880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	–1810		–1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			340	µA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	–46	–36		mA	CP to V_{IL}, Other Inputs & Outputs Open	

DC CHARACTERISTICS: V_{EE} = –4.7 to –6.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OHC}	Output Voltage HIGH	–1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to –2.0 V
V_{OLC}	Output Voltage LOW			–1595	mV		
V_{IH}	Input Voltage HIGH	–1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			–1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	–52	–40		mA	CP to V_{IL}, Other Inputs & Outputs Open V_{EE} = –6.2 V	

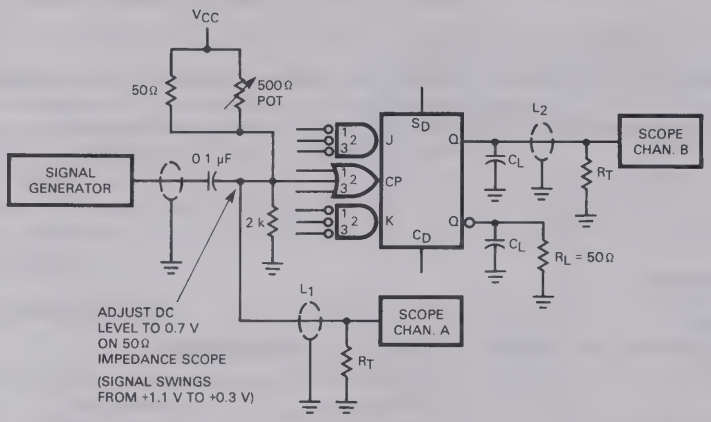
SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, T_A = 0°C to 75°C

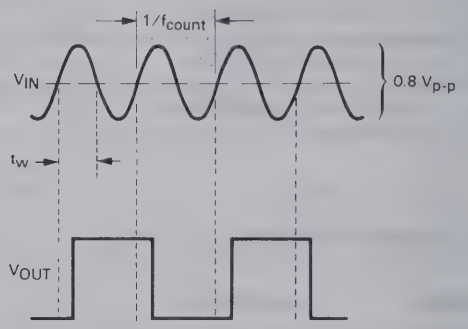
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Toggle Frequency	160	250		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output	1.6	2.8	4.4	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output	1.6	2.8	4.4	ns	
t_{PLH}	Propagation Delay S_D to Q, C_D to $\overline{Q}$	1.1	3.6	6.3	ns	See Figure 3
t_{PHL}	Progation Delay S_D to $\overline{Q}$, C_D to Q	1.1	3.6	6.3	ns	
t_{TLH}	Output Transition Time LOW to HIGH	0.9	2.0	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW	0.9	2.0	3.3	ns	

SWITCHING SET-UP REQUIREMENTS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_s	Set-up Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	See Figure 4
t_h	Hold Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	
t_w	Clock Pulse Width		2.0		ns	See Figure 1

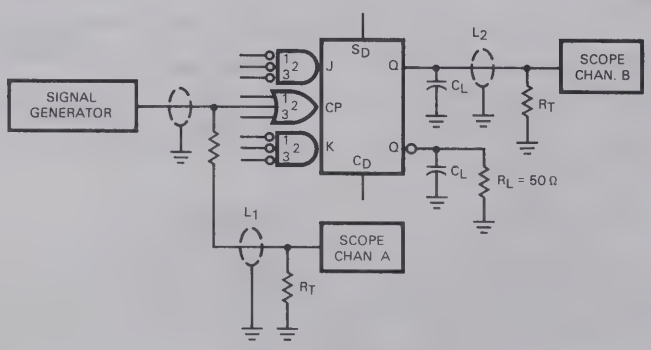
SWITCHING CIRCUITS AND WAVEFORMS

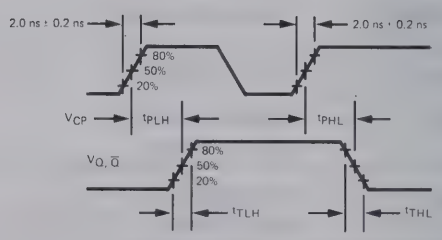




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 1. Minimum Clock Frequency

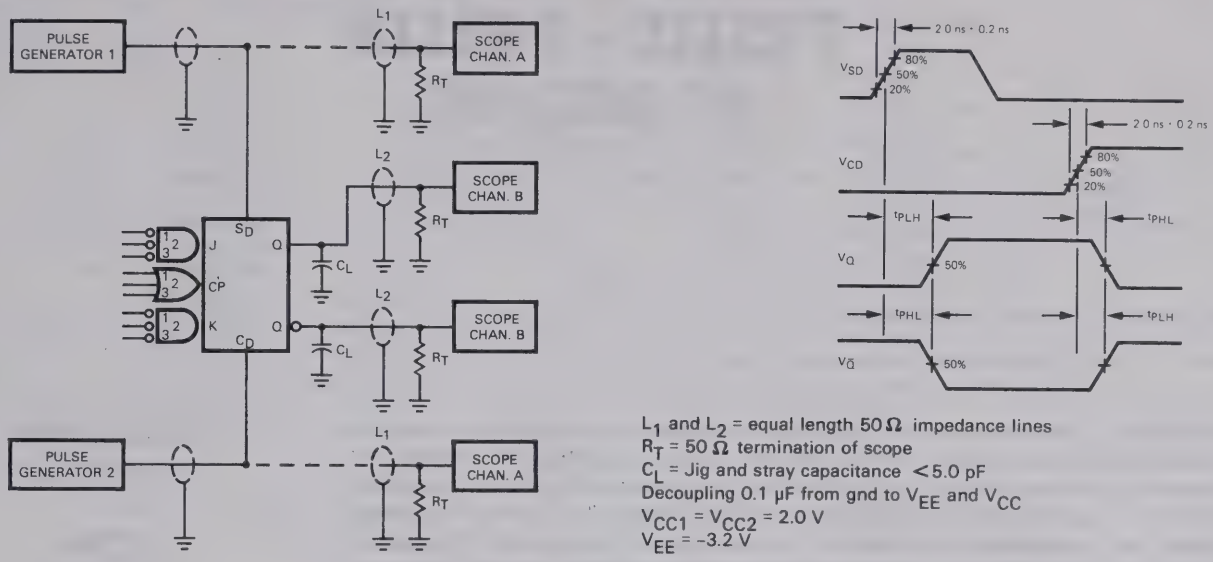




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 2. Clock Input to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 3. Asynchronous Input to Output

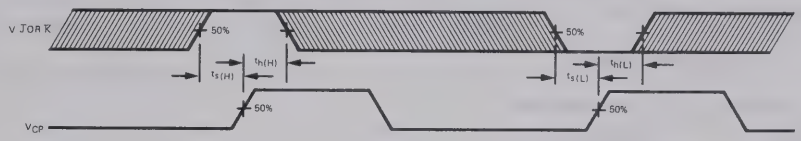
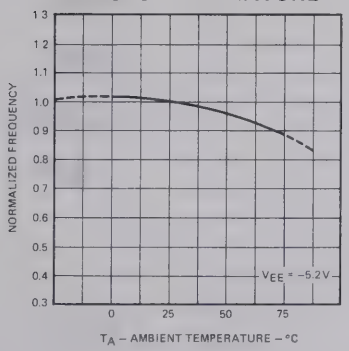


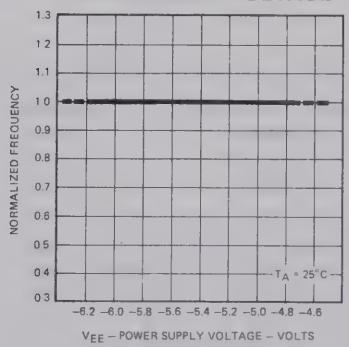
Fig. 4. Set-Up and Hold Time Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS

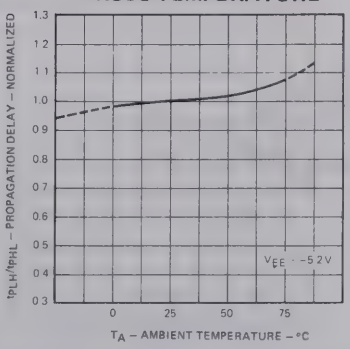
TOGGLE RATE VERSUS TEMPERATURE



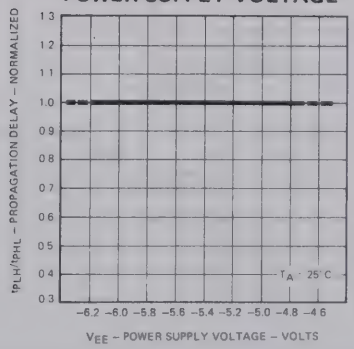
TOGGLE RATE VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS TEMPERATURE



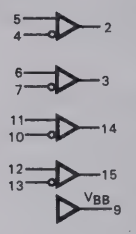
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



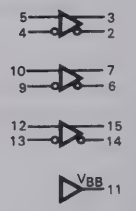
F95115 · F95116
LINE RECEIVERS

DESCRIPTION — The F95115 and F95116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide improved common mode rejection. The F95115 is a quad line receiver with single ended outputs. The F95116 is a triple line receiver with complementary outputs. The devices are voltage and temperature compensated and are fully compatible with other F95K devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high speed comparators, oscillators or broadband amplifiers.

LOGIC DIAGRAM



F95115



F95116

TRUTH TABLES

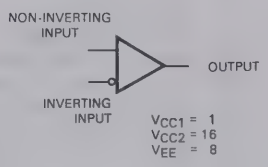
F95115 Quad Line Receiver

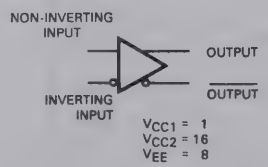
NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	H	L
V_{BB}	L	H

F95116 Triple Differential Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L

FUNCTIONS





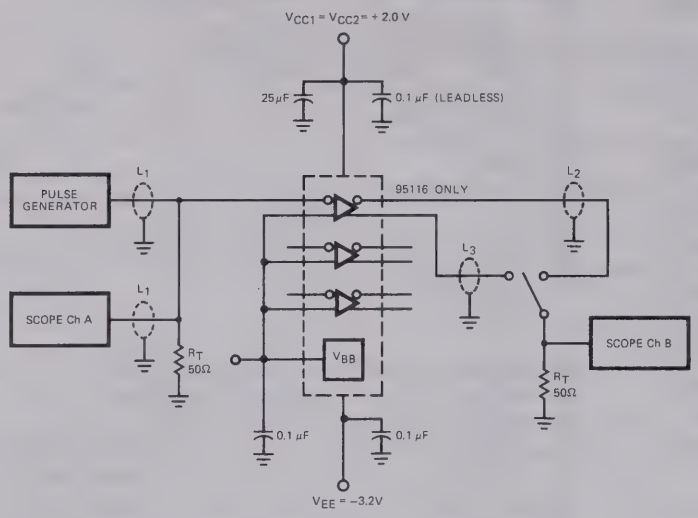
DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

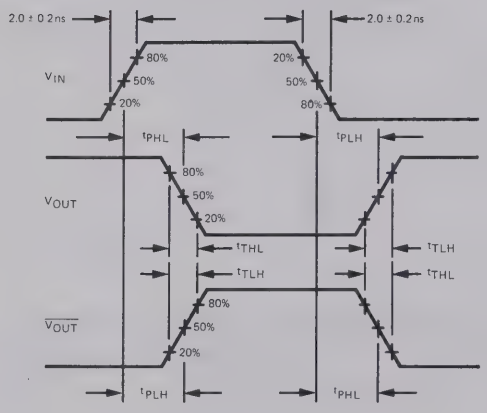
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			95	µA	$V_{IN} = V_{IHA}$	
I_{CBO}	Input Collector-Base Leakage Current	-1.0			µA	V_{IN} = -5.2 V	
I_{EE}	Power Supply Current F95115	-26	-18		mA	Leads 4,7,10,13 = V_{ILB} Leads 5,6,11,12 = V_{BB}	
	F95116	-21	-14		mA	Leads 4,9,12 = V_{ILB} Leads 5,10,13 = V_{BB}	
V_{BB}	Reference Voltage	-1380	-1320	-1260	mV	F95115,Connect Leads 5,6,11,12 to Lead 9 F95116,Connect Leads 5,10,13 to Lead 11	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0		3.1	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0		3.1	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS





Unused outputs connected to a 50Ω resistor to ground.

One input from each gate must be tied to V_{BB} during testing.

L_1, L_2, L_3 = equal length 50Ω impedance lines.

R_T = 50Ω termination of scope

Fig. 1

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor V_T may be calculated as follows:

$$V_T = \frac{(V_{EE} - V_{OH})\, R_T}{R_E + R_T + R_{LINE}}$$

Where V_{OH} is the output voltage HIGH of the driving gate, R_{LINE} is the resistance and R_T is the terminating resistor. With typical values, V_T is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between –0.55 and –3 V.

Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

TWISTED-PAIR CONNECTIONS

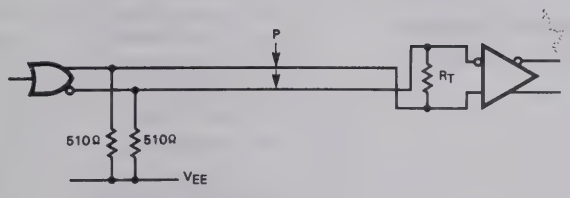


Fig. 2. Differential Transmission and Reception

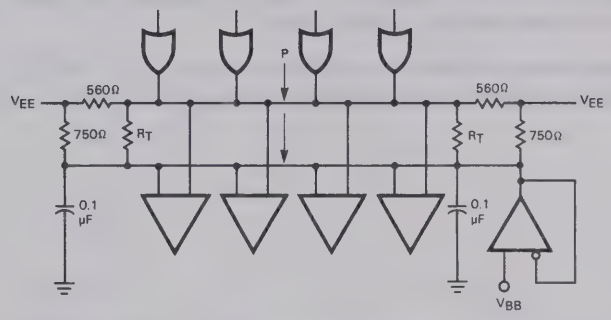


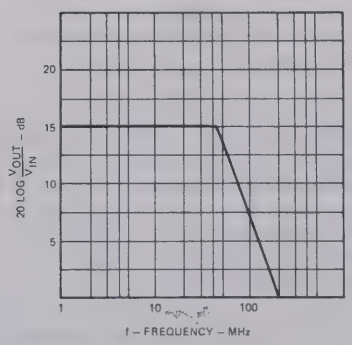
Fig. 3. Backplane Data Bus

PARAMETERS FOR LINEAR APPLICATIONS

V_{EE} = –5.2 V, V_{CC} = GND, T_A = 25°C

PARAMETER	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current	0	2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	–3.0		–0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		Vpp
Output Source Current			50	mA
Output Resistance		9		Ω

TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY



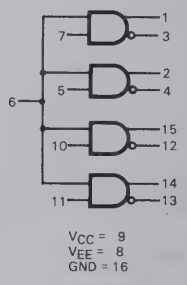
F95124

QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F95124 is a Quad Translator for converting TTL logic levels to 95K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage and temperature compensated.

When the circuit is used in the differential mode, the F95124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



Logic Equations

$2 = \overline{5 \bullet 6}$

$4 = \overline{5 \bullet 6}$

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = +5.0 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025		-880	mV	V_{IN} = +4.0 V or +0.4 V per Logic Function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810		-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	1.8		5.0	V	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	0		1.0	V	Guaranteed Input Voltage LOW for All Inputs	
V_{CD}	Input Clamp Voltage	-1.5			V	I_{IN} = -10.0 mA	
V_{BD}	Input Breakdown Voltage	+5.5			V	I_{IN} = +1.0 mA, Other Inputs V_{IN} = GND	
I_{IH}	Input Current HIGH			50	µA	V_{IN} = +2.4 V, E_C V_{IN} = +0.4 V	
I_{IHX}	Input Current HIGH E_C			200	µA	E_C V_{IN} = +2.4 V, All Other Inputs V_{IN} = +0.4 V	
I_{IL}	Input Current LOW	-3.2			mA	V_{IN} = +0.4 V, E_C V_{IN} = +4.0 V	
I_{ILX}	Input Current LOW E_C	-12.8			mA	E_C V_{IN} = +0.4 V, All Other Inputs V_{IN} = +4.0 V	
I_{EE}	Power Supply Current	-34	-26		mA	Inputs and Outputs Open	
I_{CC}	Power Supply Current		+18	+25	mA	All Inputs, V_{IN} = GND	

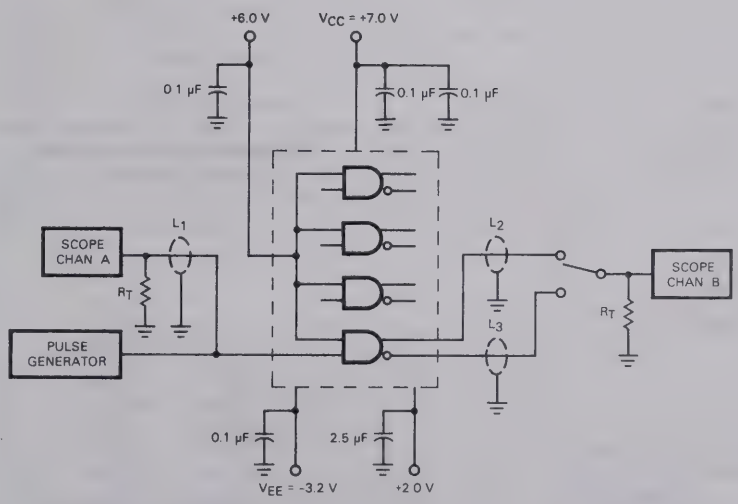
DC CHARACTERISTICS: V_{EE} = –4.7 to –6.2 V, V_{CC} = +4.75 to +5.25 V, T_A = 0°C to 75°C

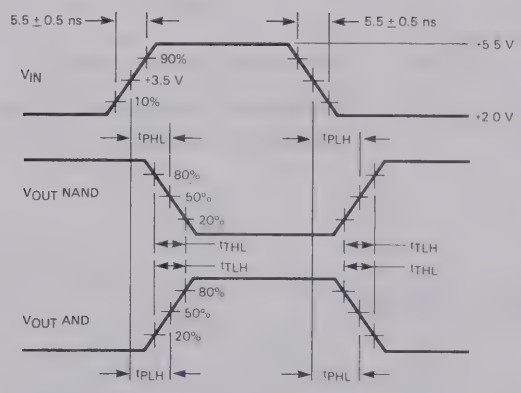
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OHC}	Output Voltage HIGH	–1050			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	Loading is 50 Ω to –2.0 V
V_{OLC}	Output Voltage LOW			–1595	mV		
V_{IH}	Input Voltage HIGH	+2.0			V	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			+0.85	V	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	–38	–29		mA	Inputs and Outputs Open, V_{EE} = –6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = +5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	3.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	3.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.9	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS





NOTES:

Connect unused outputs through 50Ω resistor to ground.
L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines.
R_T equals 50 Ω termination of scope

Fig. 1

F95130
DUAL D LATCH

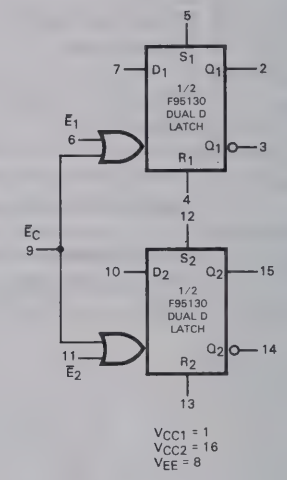
DESCRIPTION — The F95130 contains a pair of D type latches with a Common Enable ($\overline{E}_C$) input. Each latch has its own Enable ($\overline{E}_n$), Set (S) and Reset (R) inputs. For each latch, the data present on the D input appears on the Q output when both $\overline{E}_n$ and $\overline{E}_C$ are LOW, as indicated in the truth table. As long as $\overline{E}_n$ and $\overline{E}_C$ remain LOW, the Q output follows the D input signal each time it changes. When either $\overline{E}_n$ or $\overline{E}_C$ (or both) go HIGH, the latch no longer responds to changes on the D input, but retains the last valid data present at D before $\overline{E}_n$ or $\overline{E}_C$ go HIGH. The two latches can be strobed individually by using the $\overline{E}_n$ inputs, or simultaneously by using the $\overline{E}_C$ input.

The Set and Reset inputs are effective only if $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH. Note that in this mode of operation the output voltage levels of a latch are unpredictable if both the S and R signals are HIGH.

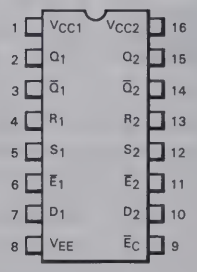
LEAD NAMES

$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
S_n	Set
R_n	Reset
D_n	Data Inputs
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

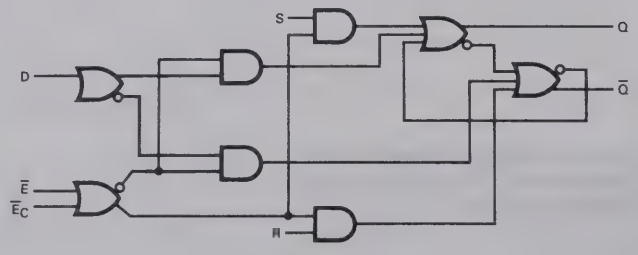
LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



(1/2 OF CIRCUIT SHOWN)

TRUTH TABLE

D	$\overline{E}_n$	$\overline{E}_C$	S	R	Q_{n+1}	OPERATION
L	L	L	X	X	L	D Function
H	L	L	X	X	H	D Function
X	H	X	L	L	Q_n	Memory
X	X	H	L	L	Q_n	Memory
X	H	X	H	L	H	Set
X	X	H	H	L	H	Set
X	H	X	L	H	L	Reset
X	X	H	L	H	L	Reset
X	H	X	H	H	-	Electrically Indeterminate
X	X	H	H	H	-	Electrically Indeterminate

L = LOW Voltage Level X = Don't Care

H = HIGH Voltage Level Q_n = Output

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025		-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810		-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH S_n and R_n $\overline{E}_n$ D_n $\overline{E}_C$			 285 220 285 265	µA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-35	-25		mA	Inputs & Outputs Open	

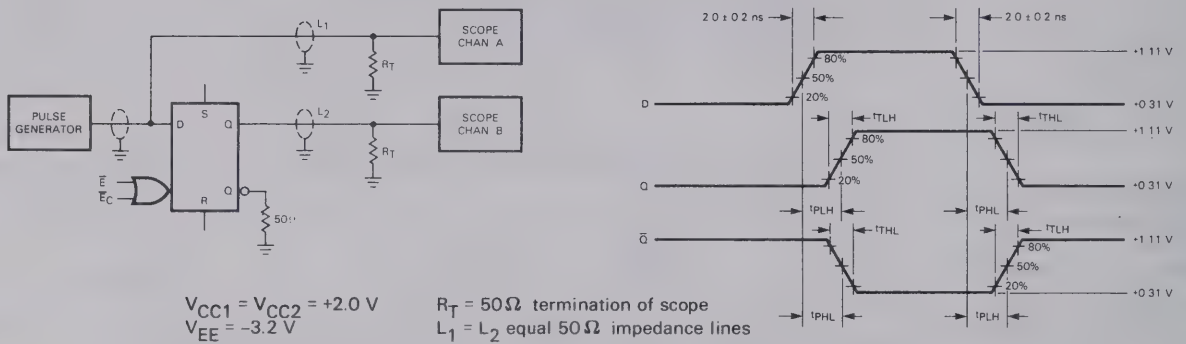
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table Loading is 50 Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV	
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs
I_{EE}	Power Supply Current	-38	-26		mA	Inputs & Outputs Open V_{EE} = -6.2 V

SWITCHING CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	See Figure 1
t_{PLH}	Propagation Delay Set to Output	1.0	2.7	3.5	ns	See Figure 2
t_{PHL}	Propagation Delay Clear to Output	1.0	2.7	3.5	ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20%–80%)	1.5	2.5	3.5	ns	See Figures 1, 2, and 3
t_{THL}	Output Transition Time HIGH to LOW (80%–20%)	1.5	2.5	3.5	ns	
t_s	Set-Up Time Data to Enable	2.5			ns	
t_h	Hold Time Data to Enable	1.5			ns	

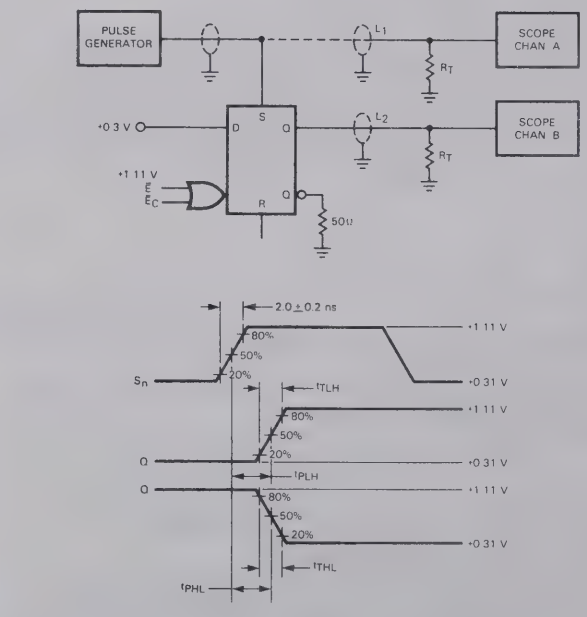
SWITCHING CIRCUITS AND WAVEFORMS



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = –3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

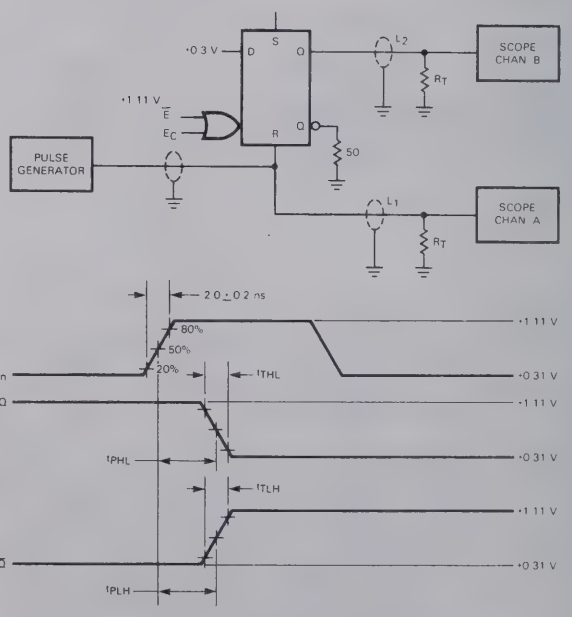
Fig. 1



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = –3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 2



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = –3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 3

F95231

HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION — The F95231 contains two master/slave D type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

LEAD NAMES

D	Data Input to Master
CP	Clock Input
CP_C	Common Clock Input
Q	Output
$\overline{Q}$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

TRUTH TABLES

SYNCHRONOUS OPERATION

D TABLE

D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

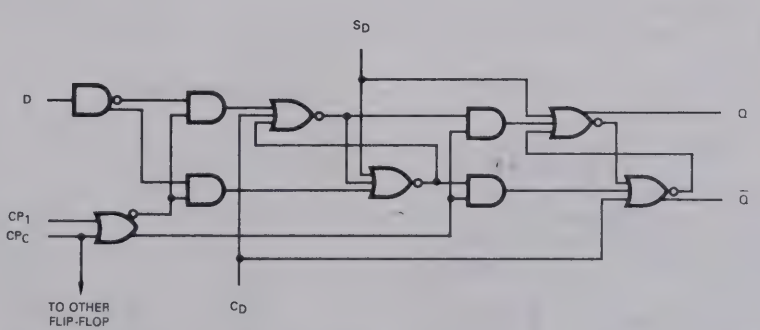
(t+1) = Time after positive going clock transition

ASYNCHRONOUS OPERATION

S_D C_D TABLE

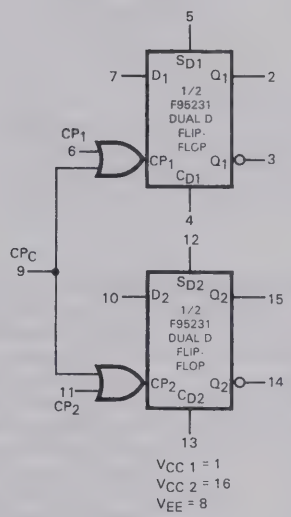
C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC DIAGRAM

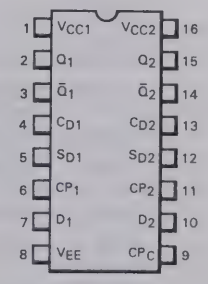


Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



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DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH				µA	V_{IN} = V_{IHA}	
	C_{D1} and C_{D2}			330			
	S_{D1} and S_{D2}			330			
	CP_1 and CP_2			220			
	D_1 and D_2			245			
	CP_C			265			
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-56	-45		mA	Inputs & Outputs Open	

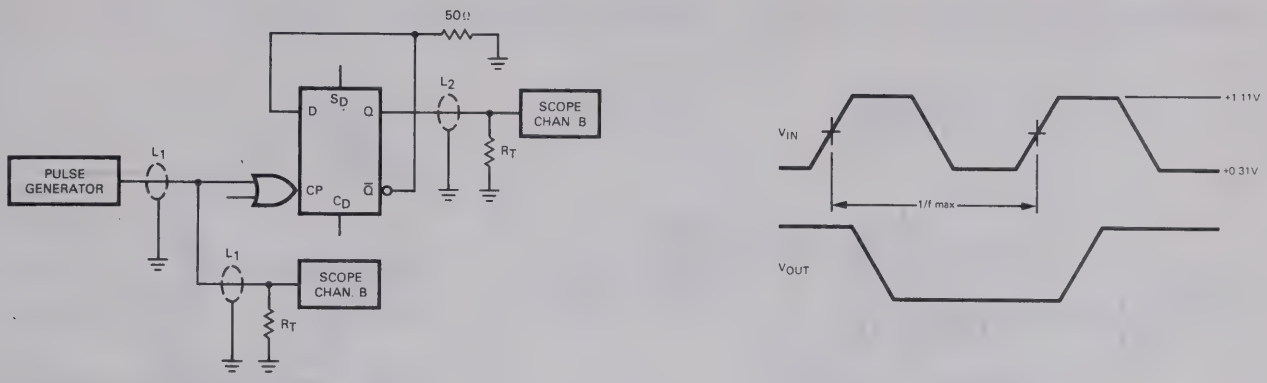
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to +75°C

V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current		-47		mA	Inputs & Outputs Open V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

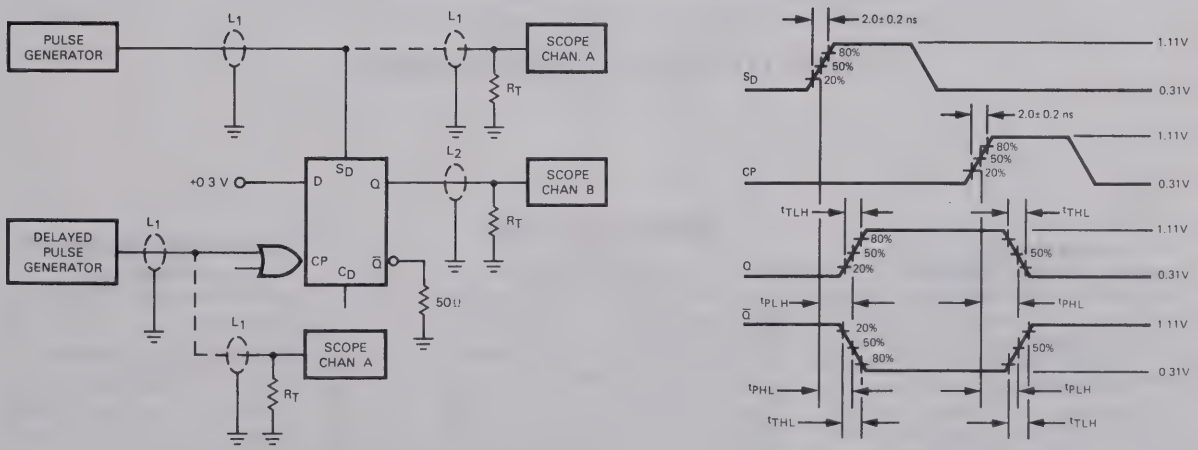
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Toggle Frequency	200			MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output	1.5	2.8	3.5	ns	See Figures 2 and 3
t_{PLH}	Propagation Delay Set to Q, Clear to Q	1.5	2.8	3.7	ns	
t_{PHL}	Propagation Delay Set to Q, Clear to Q	1.5	2.8	3.7	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.0	1.8	3.1	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.0	1.8	3.1	ns	
t_s	Set-up Time Data to Clock	1.5	0.5		ns	
t_h	Hold Time Data to Clock	0.75	-0.5		ns	

SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

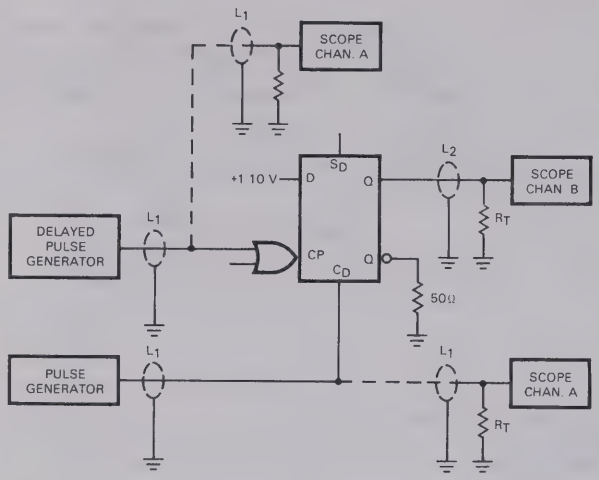
Fig. 1. Toggle Rate Test Circuit and Waveforms

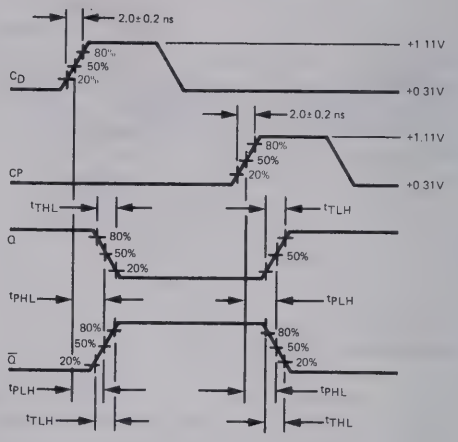


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Propagation Delay and S_D Test Circuit

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)



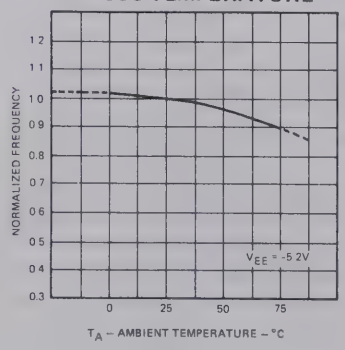


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

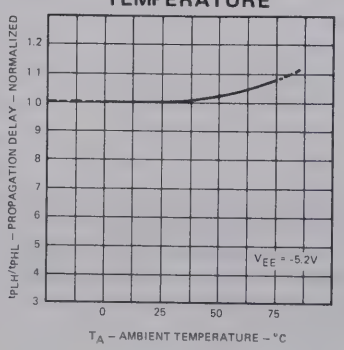
Fig. 3. Propagation Delay and C_D Test Circuit

TYPICAL ELECTRICAL CHARACTERISTICS

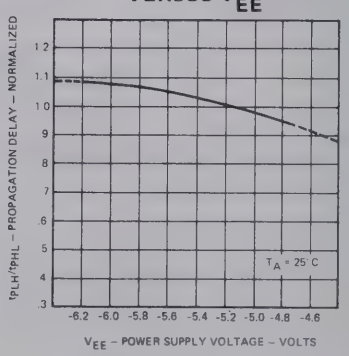
TOGGLE RATE VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS TEMPERATURE

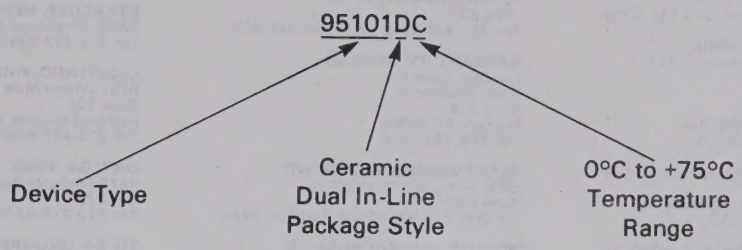


PROPAGATION DELAY VERSUS V_{EE}



ORDERING AND PACKAGE INFORMATION

The order code format and correct ordering codes for the products described in these data sheets are as follows:

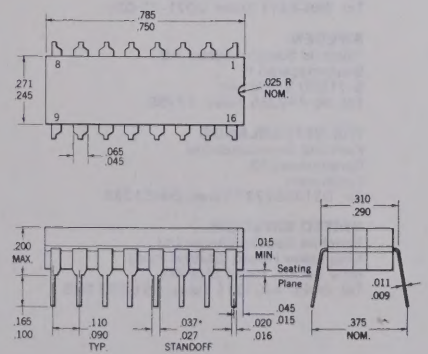


ORDERING CODE	DESCRIPTION
95000DC	4-Bit Shift Register
95002DC	Dual 4-Input OR/NOR Gate
95003DC	Triple 2-Input OR/NOR Gate
95004DC	Quad 2-Input NOR Gate
95010DC	BCD Decade Counter
95016DC	4-Bit Binary Counter
95029DC	Edge Triggered $\overline{JK}$ Flip-Flop
95101DC	Quad OR/NOR Gate with Common Enable
95102DC	Quad 2-Input NOR Gate
95103DC	Quad 2-Input OR Gate
95105DC	Triple 2-3-2-Input OR/NOR Gate

ORDERING CODE	DESCRIPTION
95106DC	Triple 4-3-3-Input NOR Gate
95107DC	Triple Exclusive OR/NOR Gate
95109DC	Dual 4-5-Input OR/NOR Gate
95110DC	Dual 3-Input/3-Output OR Gate
95111DC	Dual 3-Input/3-Output NOR Gate
95115DC	Quad Line Receiver
95116DC	Triple Line Receiver
95124DC	Quad TTL to ECL Translator
95130DC	Dual D Latch
95231DC	High Speed Dual D Flip-Flop

PACKAGE OUTLINE

16-Lead DIP



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
* The .037/.027 dimension does not apply to the corner leads

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